Silicon Solar Cells

1. Fabrication of a novel solar cell with 3-D junction

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The main objective of the study is to achieve very deep junction in silicon using laser doping/laser assisted diffusion and use such feature in alternative solar cell structure. The cell structure would allow the collection of carriers laterally thus reducing the requirement for high carrier lifetime if designed properly. The current research direction in this work is to use different alternative techniques to measure the junction depth after laser assisted diffusion and thus optimize the annealing process.

The dopant depth profiling of Phosphorous in sample prepared by laser doping was done using Glow Discharge Mass Spectroscopy (Thermo Fisher Scientific). The concentration vs. depth profiles are presented in Fig. 1. The dopant atoms have been diffused to a depth up to 14 µm by laser induced melting and melt phase diffusion. In the earlier reports, we had presented data which gave estimation of junction depth using alternative or indirect methods. The depth profiles clearly show deep diffusion of P as expected from the process. Depth profiling was done on two different locations on same sample (13-09-12). The sputtering in ‘spot 2’ overlapped partially with undoped region of the sample. Hence the difference in depth profiles is expected to be an error coming from this experimental misalignment. The depths were measured using surface profilometer.

![Fig. 1: Phosphorous depth profiles measured using Glow Discharge Mass Spectroscopy (GDMS).](image1)

![Fig. 2: SEM – EBIC measurement (TIFR, Mumbai) after laser doping. The left cursor was placed at the surface of the sample as seen from SEM image while the right cursor is positioned at the peak of the current.](image2)

Fig. 2 represents the depth of junction after laser doping. The glow occurs due to electron beam induced current. The measurement was done in SEM-EBIC (Zeiss) at TIFR, Mumbai. The measured junction in this image from the top-surface is 6.1 µm. The depth is relatively smaller as compared to GDMS data shown above. The sample preparation was different in this case which may have affected the results. Modification in sample preparation will be done to obtain better images from this measurement.

Two different pulse repetition rate (PRR) or frequency and three different scan speeds were used to fabricate samples for depth profiling. Time plasma profiling TOF-MS (PPTOFMS, Horiba Scientific) was used for depth profiling. The PPTOFMS works on principles almost similar to GDMS, where ions from Ar plasma sputter the surface and the secondary ions from samples is analyzed through a TOF-MS. Fig. 3(a) and Fig. 3(b) depicts the depth profiles for two different PRR. As the scan speed reduces, the retention time of the laser increases and, thus, leads to formation of a deeper junction. Our earlier observation of same trend of junction depth estimated by selective etching is thus established. It can be observed comparing the two figures that with lower PRR for both 10 mm/s and 20 mm/s, junction depths are increased. However, this observation is not well understood and is being studied through the optimization processes.
EBIC measurement (TIFR, Mumbai) on the cross-section was done on different samples to measure the junction depths under different conditions. Fig. 4 is a representative superposition of SEM image and corresponding EBIC signal maps. The superposition was done in a post-processing step using 'ImageJ' software as the SEM-EBIC systems do not have an in-built software tool for the same. In case of EBIC measurements, two-step diffusion was performed as it is required. First diffusion was done to make a surface emitter. Second step was performed like a selective emitter with laser doping conditions that can lead to deeper junctions.

Fig. 4: Representative SEM-EBIC superposition image (TIFR, Mumbai). The superposition was done in a post-processing step using ‘ImageJ’.

Fig. 5 represents the sheet resistance measured for different pulse lengths of the laser with fixed PRR and speed. With increase of the pulse length, the sheet resistance reduces and it again indicates formation of a deeper junction. EBIC measurements were done to understand the same. Fig. 6 depicts the values of junction depth measured from EBIC.

Fig. 5: Variation of sheet resistance with pulse duration at 10 kHz and 40 mm/s.

Fig. 6: Junction depth measured using EBIC for different pulse duration. However in this case two-step diffusion was used.
2. Novel technologies for contact formation using temperature sensitive paste

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Commercially available solar cells are patterned using screen-printing technique to make contacts at front side with silver containing metal paste. Screen printed solar cells have average finger widths of 80 - 100 µm which result in significant losses due to shading. We propose the use of a temperature sensitive paste for the realization of metal contacts with narrow width. The progress made during the year under review is summarized below.

Chemical etching method by electro-discharge machine (EDM) wire is performed on ARC of half-finished solar cells. Finger opening width of 47 µm were achieved using 30 µm, and 87 µm are achieved using 50 µm EDM wires. Since the EDM wire patterning manual method has limitations in continuity and finer finger widths, the experimental procedure is slightly modified.

A novel design for patterning of AR coatings using mechanical structure is designed. Also, using EDM wires the patterning mechanism is performed. Very fine finger widths are obtained using EDM wires. Wide variety of EDM wires are used to pattern range from 30-100µm. Using this design, continuous fingers could not be printed due to wire alignment. Continuity in a printed line is required for the patterning of solar cells. For this, a new set up is designed.

A spool of EDM wire is kept in the top left wheel in the design as shown in the Fig. 7. From this, the wire passes to the bottom left wheel and paste container. Sufficient amount of etch paste is kept in the paste container. 0.5 mm diameter nozzle is kept outside the paste container through which, the wire comes out and passes through bottom right wheel. Top right wheel is the end position for the wire which will drive all the wheels using electric motor with 10 rpm. Paste containing wire comes out of the container will be used for printing lines on solar cell. Exactly below the paste contained wire, the solar cell with pre heated condition is

![Fig. 7: Patterning by EDM wire mechanism using Newport 3D stage setup which contains paste container, EDM wire, solar cell and heating setup.](image-url)
kept and using z-axis the wire is kept in contact with the solar cell. Paste contained wire contacts the solar cell and paste is transferred to it in continuous line form. Ultimately this is heated to 390°C. Again, the driving motor will pull the wire from the spool for the next printing. After single print, using x-axis in 3D stage, the cell is moved to next printing position accurately. Hence, continuous lines are printed with equal distance of separation on the solar cell. The cell is in heated condition until all the lines are printed on it. The process sequence for printing is moving down the z-axis for contacting solar cell, moving up the z-axis, moving spool of printed wire by driving motor for next printing, moving x-axis for next print line. In this process, the z-axis may be sufficient of greater than required. To optimize this, the exact value is to be calculated by varying different positions.

The paste wire exactly touches the solar cell is noted as zero distance (snap-off). From this, the snap off increased in 0.1, 0.2, 0.3, 0.4 mm respectively and contacted the solar cell. Using each snap off distance, 4 continuous lines are printed and linewidths are measured and plotted the max, min and average of finger width after etching in Fig. 8.

![Fig. 8: Maximum, minimum and average finger width of five different snap off distances for all printed lines.](image)

With a fixed velocity (50 mm/sec), all the lines are printed with same conditions using 40 μm molybdenum EDM wire. The cell is pre heated to 390°C. The snap off distance is varied in steps of 0.1 mm from 0 to 0.4 mm. From the above graphs, at 0 to 0.4 mm, the optimum is appearing at 0.2 mm of snap off distance. For reduction in finger width, optimum snap off distance is required. The fine finger width along with continuous fingers can be achieved at optimum snap off distance.

Once, the cell is printed with required number of fingers, it is rotated in 90° C for the bus bar printing. The bus bar is also implemented once the finger lines are continuous.

### 3. Plasmonics for Photovoltaic Applications

**Students:** Hemant Kumar Singh  
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In the process of optimizing (minimization) the reflectance from the front surface we are exploring the plasmonics technology by using metal nanoparticles on the front of the substrate in order to utilize the plasmonics assisted enhanced forward scattering. We explored initially many device structure suitable for such condition and then we started the optimization of nanoparticles fabrication.

We have shown in earlier report that we are able to minimize the reflection from sandwiching the Ag film which results in better trapping of light and hence reduced reflection in UV-Vis region however in IR region this shows still relatively higher reflection. In order to get better broadband (300–1200 nm) anti reflection property from sandwiched structure, we did some optical simulation to get optimum thickness and RI for dielectric and
metal before fabrication of the device for which the results are briefly given here. For finding the optimum thickness of intermediate metal layer for dielectric-metal-dielectric device geometry, we used multilayer device geometry for simulation and estimated that Ag ultra thin films of thickness 5-10 nm is promising for such geometry. For comparative study we used weighted reflection weighted with respect to AM 1.5G for different metal and dielectric material thickness and refractive index (RI). For finding the optimum top and bottom ARC thickness, we calculated weighted reflectance for SiNx bottom layer with RI 1.99 and top layer SiNx with RI 1.92 and silver ultra thin film intermediate layer thickness of 5 nm. We did simulation for different top and bottom layer thickness. The device geometry used for simulation is shown in Fig. 9(a). Fig. 9(b) shows the contour plot for calculated weighted reflectance (WR) for broad wavelength range (300 nm-1200 nm) for such device geometry.

![Fig. 9: (a). Device geometry under study (Si-SiNx-Ag-SiNx) (b). Contour plot for weighted reflectance for different top and bottom layer thicknesses for 5 nm of silver ultra thin film intermediate layer.](image)

It was observed that for such multilayer geometry, 120 nm bottom and 40 nm of top SiNx layer will be optimum for 5 nm of Ag ultra thin film intermediate layer for which the weighted reflectance (WR) was estimated around 12.5 %. Also for this 120 nm bottom SiNx and 40 nm top SiNx layer with 5 nm Ag intermediate layer, we simulated the reflectance for different RI for top and bottom SiNx dielectric layers which is shown in Fig. 10(a). This suggest that for such device geometry the bottom layer dielectric RI is crucial irrespective of top layer RI provided the top dielectric layer RI is less or equal to bottom layer dielectric RI. For such given case if the bottom dielectric layer RI is between 2.03 -2.15, the calculated RI is much lesser and for bottom dielectric layers with RI 2.15, if top layer RI is 1.99, this gives only 10.7 % WR whereas the same structure without Ag intermediate layer gives 18.9 %. Fig. 10(b) shows the simulated reflectance plot for best device geometry Si/SiNx(120nm)/Ag(5nm)/SiNx(40nm) along with experimental data plot as well as simulated reflectance data for our previously fabricated device geometry Si/SiNx(60nm)/Ag(9nm)/SiNx(40nm). Please note that here in these simulations only multilayer thin film interference based optical simulation is done and no plasmonic effect has been considered. But in actual scenario for such cases plasmonic effect will play a crucial role which will be seen once we will be fabricating the actual device. We expect the calculated WR to be less i.e. much better ARC property as this can be seen from Fig. 10(b) where the simulated reflectance predicted
the weighted reflectance to be 28.3 % whereas actual was observed around 10.9 % for Si/SiNx(60nm)/Ag(9nm)/SiNx(46nm) which is due to plasmonic effect of intermediate layer. As now we have best optimized multilayer geometry, our next step is to fabricate and we expect to get much better total weighted reflectance (TWR) as seen for previously fabricated sample Si/SiNx(60nm)/Ag(9nm)/SiNx(46nm) where experimental TWR (TWR: 10.9 %) was much lesser than simulated weighted reflectance (WR: 28.3 %).

Based on the above simulation results, we optimized further the dielectric-metal-dielectric sandwiched structure. Here we used Ag ultra thin film sandwiched in SiNx top and bottom layer on p-type Si substrate. The device geometry used for fabrication is shown in Fig. 11 (a). Fig. 11 (b) shows the cross sectional SEM image of the best sample based on dielectric-metal-dielectric (D-M-D) plasmonic ARC structure.

It is observed that for such multilayer geometry, 80 nm bottom and top SiNₓ layer with 8 nm of Ag ultra thin film intermediate layer, the weighted reflectance (WR) is minimum for broad wavelength range 300 nm - 1200 nm. It is calculated around 8.1 % which is 41 % lesser than standard 80 nm SiNx based ARC geometry which is in the range of 13.8 %. Also for this, the anti-reflection property in infrared wavelength region is much better than previously fabricated device structure. The total reflectance plot is shown in Fig. 12(a) for Si/SiNₓ(80nm) and the best sample Si/SiNₓ/Ag-UTF/SiNₓ (Plasmonic ARC D-M-D structure). Fig. 12(b) shows the weighted total reflectance bar plot for standard 80 nm based ARC structure i.e. Si/SiNₓ(80nm) and the best sample Si/SiNₓ/Ag-UTF/SiNₓ (Plasmonic ARC D-M-D structure). It is clear from the Fig. 12(b), the D-M-D structure improves the anti-reflection property both in UV-Vis as well as infrared wavelength range. For 80 nm SiNₓ based D-M-D structure the TWR for UV-Vis wavelength range was 10.1 % compared to 13 % for standard 80 nm SiNₓ based ARC structure. Also the most reasonable improvement is seen in infrared wavelength range while maintaining the lower reflection in UV-Vis wavelength range as TWR as low as 5.5 % is observed for IR range (700nm -1200nm) which was 14.7 % for standard 80 nm SiNₓ based ARC structure.

Fig: 11: (a) Device geometry under study (Si-SiNx-Ag-SiNx) (b) Cross sectional image of best sample based on dielectric-metal-dielectric (D-M-D) plasmonic ARC structure.

Fig: 12: (a) Total reflectance plot for Si/SiNₓ(80nm) and the best sample Si/SiNₓ/Ag-UTF/SiNₓ (Plasmonic ARC D-M-D structure) (b) Weighted total reflectance (TWR) bar plot for standard 80 nm based ARC structure i.e. Si/SiNₓ(80nm) and the best sample Si/SiNₓ/Ag-UTF/SiNₓ (Plasmonic ARC D-M-D structure). Back colour bar represents the calculated TWR for wavelength range 300 nm -1200 nm; Red colour bar represents the calculated TWR for wavelength range 300 nm -700 nm (UV-Vis range); Blue colour bar represents the calculated TWR for wavelength range 700 nm -1200 nm (Infrared range).
Ag ultra thin film sandwiched in SiN, top and bottom layer i.e. plasmonic antireflection layer on p-type Si substrate based solar cell is realised. The device geometry used for fabrication is shown in Fig. 13(b). Fig. 13(a) shows the device geometry for PV cell without plasmonic antireflection layer. For all devices planer (non-textured) surface were used.

Fig. 13: (a). Device geometry for PV cell without sandwiched structure (b). PV cell with dielectric-metal-dielectric (D-M-D) plasmonic ARC structure.

The PV cell was fabricated using ascut (non-textured) surface based wafers which were 180 micron thick and base resistivity of 1 ohm-cm. After diffusion the sheet resistance measured and found to be 44 ± 3 ohm/sq. For non-plasmonic ARC layer based PV cell, SiN ARC thickness used was 80 nm and for D-M-D structure, it was as optimised 80 nm-8 nm-80 nm. It is observed that for such multilayer geometry, 80 nm bottom and top SiN layer with 8 nm of Ag ultra thin film intermediate layer, the weighted total reflectance (TWR) is 9.1 % for broad wavelength range 300 nm - 1200 nm which is lesser than standard 80 nm SiN based ARC geometry which results 13.6 %.

The EQE and IQE characteristics of these cells are shown in Fig. 14. Reasonable improvement is seen in EQE for Plasmonic ARC based device structure when compared to standard SiN ARC based device on non-textured based solar cells. However the effect high reflection region as seen in visible region in reflectance curve can be seen in EQE of the device. Also some parasitic absorption is there (Fig. 14(b)) which is to be further minimized.

Fig. 14: (a). EQE graph plot for solar cell with standard ARC (PV-1) and solar cell with D-M-D plasmonic ARC (PV-2); (b). IQE graph plot for PV-1 and PV-2.

The dark and light I-V of the two cells are shown in Fig. 15. There is slight improvement in current generation as seen in light I-V curve (Fig. 15(b)) is due to improved anti-reflection from D-M-D structure The cell parameters extracted are listed below in table 2.

Table 2: Extracted solar cell parameter form Light IV curve

<table>
<thead>
<tr>
<th>Sample</th>
<th>Area (cm²)</th>
<th>Vmp (mV)</th>
<th>Impp (mA/cm²)</th>
<th>Vmp (mV)</th>
<th>Impp (mA/cm²)</th>
<th>Rs (ohm-cm²)</th>
<th>Rsh (ohm-cm²)</th>
<th>FF (%)</th>
<th>η (%)</th>
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<tr>
<td>PV-1 (Std 80 nm SiN ARC)</td>
<td>11.2</td>
<td>614.5</td>
<td>34.73</td>
<td>522.0</td>
<td>32.08</td>
<td>980</td>
<td>1.32</td>
<td>78.49</td>
<td>16.75</td>
</tr>
<tr>
<td>PV-2 (D-M-D Plasmonic ARC)</td>
<td>15.2</td>
<td>616.3</td>
<td>34.86</td>
<td>526.4</td>
<td>32.29</td>
<td>1010</td>
<td>0.98</td>
<td>79.12</td>
<td>17.00</td>
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</table>
In summary we have fabricated PV cell with optimized anti-reflection property using dielectric-metal-dielectric structure on non-textured Si substrate with weighed total reflectance of 9.1% for broad wavelength range 300 nm -1200 nm along with improved I-V curve and relative efficiency improvement. Though there is comparatively a bit high reflection in visible region, the efficiency of the plasmonic ARC based device (PV-2) was improved to 17%, i.e. 1.5% relative efficiency improvement is shown as the base device (non-textured PV cell with std SiN₅ ARC) efficiency was 16.75%. Our next focus is to minimize further the anti-reflection property in UV-Visible region and the base PV cell efficiency and the comparative efficiency enhancement.

4. Slicing of silicon wafers for PV applications using Wire Electric Discharge Machining (WEDM)

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Faculty members: Suhas S. Joshi

Wire- Electro-Discharge Machining (EDM) used extensively primarily in automobile, tool, die, and mould making industries. This study gives (a) simulation of the wire EDM process (b) process optimization and (c) damage studies.

Wire Vibration Model:
The wire tool in WEDM can be modelled as a vibrating string, fixed at both its ends. A blockdiagram describing the model inputs and outputs is shown in Fig. 16 below. Thus, the governing differential equation for the vibration of the wire:

\[ T \frac{\partial^2 y}{\partial z^2} - \mu \frac{\partial y}{\partial t} + F_z(z,t) = \rho \frac{\partial^2 y}{\partial t^2}, \]

where:
- \( T \): Wire Tension
- \( \mu \): Viscosity of dielectric medium, and
- \( \rho \): linear mass density of wire, i.e.

Equation can be solved for the boundary conditions:
\[
\begin{align*}
    y(0,t) &= 0 \\
    y(l,t) &= 0
\end{align*}
\]

and the initial conditions:
\[
\begin{align*}
    y(z,0) &= 0 \\
    \frac{\partial y}{\partial t}(z,0) &= 0
\end{align*}
\]

The maximum amplitude of the wire obtained is thus:
\[
A = 4F_0 \sum_{n=0}^{\infty} \frac{1}{\sqrt{4n^2T^2 + \mu^2T^2}} e^{-\frac{n^2\lambda^2}{4P}}.
\]
Where $F_0$ is the magnitude of the spark force. The maximum amplitude of wire vibration is, thus, found to depend on the wire tension, wire linear mass density, the distance between the wire guides and the viscosity of the dielectric medium. The magnitude of the spark force is required to calculate the wire vibration amplitude. The effect of varying different process parameters on amplitude and frequency is described in the following sections.

The effect of varying different process parameters on amplitude and frequency is described in the following sections.

The variation of vibration amplitude with wire tension is shown in Fig. 16. It can be seen that the amplitude of vibration varies inversely with wire tension. Varying the wire tension can be used to reduce the vibrations and consequently, the change in width of cut caused by the vibrations.

It is observed that the amplitude of vibrations increases with an increase in current and voltage (See Fig. 16 and Fig. 17). This is because either a greater voltage or current leads to an increase in the amount of energy released in every pulse which increases force causing vibrations.

The variation of the principal frequency of wire vibrations with tension and the distance between wire guides has also been calculated from the model (See Fig. 18 and Fig. 19). Although the distance between wire guides does not directly influence the width of cut, it is an important quantity in understanding the vibration behavior of the wire in WEDM. The relation between the wire vibration frequency and the distance between the wire guides and the temperature distribution in the wire and workpiece. The variation of vibration frequency is found to affect the vibration frequency much more as compared to the variation in the distance between the wire guides.

The width of cut has been calculated using the model. The value for spark gap is held constant at 10 µm. The variation of the width of cut for different values of wire tension and open circuit voltage has been plotted (See Fig. 20). The linear variation of the width of cut with amplitude of vibrations is observed. The wire tension is observed to be the most significant parameter affecting the width of cut and is responsible for an increase of almost 3% in width of the cut.

| Fig. 16: Variation of maximum wire vibration amplitude with wire tension. | Fig. 17: Variation of maximum wire vibration amplitude with discharge current. |
| Fig. 17: Variation of maximum wire vibration amplitude with open circuit voltage. | Fig. 18: Variation of wire vibration frequency with wire tension. |
| Fig. 18: Variation of wire vibration frequency with wire tension. | |
During the year under review we have installed a new wire EDM machine. The process parameters for slicing wafers are being optimized. Experiments were carried out to find the slicing speed of ultra thin silicon wafer by wire-EDM and study its thickness variation, surface roughness and sub-surface damage. The definition of the dimensions of the wafer are shown in Fig. 21.

Cutting wire:  
- a. Material: Brass,  
- b. Diameter: 100 µm,  
- c. Polarity: Negative  
Cutting parameters: The cutting parameters are adjusted such that while cutting the breakage of wire and wafers does not happen and the target was to achieve the minimum wafer thickness.

Table 3: Wire EDM process parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>L1</th>
<th>L2</th>
<th>L3</th>
<th>L4</th>
<th>L5</th>
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<tr>
<td>Open Voltage (Volts)</td>
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<td>65</td>
<td>68</td>
<td>71</td>
<td>74</td>
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<tr>
<td>Servo Voltage (Volts)</td>
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<td>39</td>
<td>41</td>
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<td>45</td>
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<tr>
<td>Pulse on time (µs)</td>
<td>0.3</td>
<td>0.4</td>
<td>0.5</td>
<td>0.6</td>
<td>0.7</td>
</tr>
<tr>
<td>Pulse off time (µs)</td>
<td>7</td>
<td>9</td>
<td>11</td>
<td>13</td>
<td>15</td>
</tr>
</tbody>
</table>

Response surface methodology was used with central composite design (4 centre points) to design the experiments. Twenty eight experiments were performed repeating each experiment two times.

**Slicing Rate**

\[-6.00442 + (0.080036 \times OV) + (0.080036 \times SV) + (5.21134 \times Ton) + (0.26985 \times Toff) - (0.078497 \times OV \times Ton) - (6.51e-3 \times SV \times Toff)\]
It was observed that:

a. With an increase in open voltage slicing rate (SR) was increasing.
b. With an increase in servo voltage slicing rate was decreasing.
c. No effect of pulse on and off time was seen on slicing rate.

Interaction plots between various process parameters are shown in Fig. 23.

The wafer thickness: The sliced wafer was divided into three regions as shown in Fig. 24(a). i.e. entry region, central region and exit region based on the travel of the wire. The wafer thickness was measured for each and every wafer and the effect of cutting parameters were studied for all the three regions. The results are summarized in Fig. 24.
The maximum wafer thickness was obtained at the entry region, and the minimum wafer thickness was at central region. This can be attributed due to wire vibration effects at central region. A decrease in wafer thickness was seen with increase in servo voltage and pulse on time. No significant change in wafer thickness was seen with change in open-voltage and pulse on time.

Surface roughness and the damage that causes it are important parameters for the eventual wafers sliced using the process. We have investigated surface roughness on W-EDM sliced silicon wafers.

**Estimation of surface roughness:**

Surface roughness(\(\mu m, Ra\)) = -20.0213 + 0.425116*OV + 0.204806*SV + 11.9927*Ton - 0.178241*Toff - 0.00119954*OV * OV + 0.00265521*Toff * Toff - 0.236944*OV * Ton + 0.00322222*OV* Toff + 0.160000 *S *Ton - 0.210625 * Ton * Toff

The parametric dependence is obtained using regression analysis and the goodness of fit is estimated at 92%, indicating a fairly good fit. The dependence of various process parameters, obtained from the fitting process are shown in Fig. 25.

The problem of finding an optimum solution for process parameters is a multi objective optimization problem. The solution is shown in table 4. Fig. 26 shows the optimality plot of the optimization problem.
Thermal damage on the surface:

SEM images were taken on the wafer surface and along the edge of the wafers (Fig. 27) to see the wire-EDM cutting on the wafer surface and depth of damage due to thermal process. The depth of thermal damage is the physical damage obtained from SEM plots and quantification of depth of damage on the wafer surface has been done by measuring thickness of disturbed layer on a wafer surface.

The marks made by wire during cutting were seen at a magnification of 160 X (Fig. 27(a)). The craters formed and the recast layer during machining are shown at a magnification of 1400 X (Fig. 27(b)). Thermal damage study was done at three different places along the edge of the wafers as shown in Figure 4. It was found that an average of 11µm layer was found in the thermal damage. No sign of any type of cracks were seen on the wafer surface.
Fig. 27: SEM images showing wire saw marks (a) and crater size on the wafer surface, (b).

Fig. 28: SEM images showing thermal damage on the wafer edge at three different locations on the wafer.