2. High Efficiency Crystalline Si Solar Cells


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The target and timelines for this deliverable are shown in Fig. 2.1.

![Fig. 2.1: Targets and timelines for high efficiency solar cells. Present status is 14.9% efficiency on p-type c-Si.](image)

Achievements during the year under review (2nd year) in comparison to the status at the end of the first year are shown in the table below.

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<td>Boron rich layer with islands on the surface seen for spin-on-dopant</td>
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<td>Al2O3 deposited by pulsed DC sputtering was shown to result in a surface recombination velocity of 1080 cm/sec</td>
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Cell fabrication and results:

In the previous year, we reported cells with 13.2% efficiency. These cells implemented phosphorus doped emitters, device separation by oxide grown in the wet ambient, Ti/Pd/Ag front contacts, thermally stable SiNx:H anti-reflective coating, and Al back contacts. The front surface was not textured. During the last one year, a thermally stable passivation layer has been developed as well as to give the optimum anti-reflection property. A bilayer anti-reflective coating has been implemented in the subsequent run, and the solar cell exhibited $V_{oc} = 590 \text{mV}$, $J_{sc} = 39.5 \text{mA/cm}^2$, $FF = 64\%$, and efficiency = 14.9%. The process flow used for fabrication and the IV characteristics of the champion cell are shown in figures 2.2 and 2.3 respectively. Except for the FF all other parameters have shown significant improvements over previous year. Contacts are currently being optimized to address two issues: (i) reduce contact resistance and sheet resistance (ii) deposition of thick metal layers for compatibility with textured surfaces of the solar cells. With the integration of texturing process, back surface field and thick metal contacts with low contact and sheet resistances and high shunt resistance, we hope to achieve 18% efficiency by the end of the third year.

![Fig. 2.2: Process flow used for fabrication of the champion cell.](image1)

![Fig. 2.3: IV characteristics of the champion cell under one sun illumination.](image2)

The cell process reported in the previous year was used for developing a selective emitter cell process. The process flow is shown in Fig. 2.4. Cells were fabricated with boron back surface field, phosphorus doped selective emitter, oxide/SiNx ARC stack, Ti/Pd/Ag front contacts, and Al back contacts. The front surface was non-textured as contact deposition by physical vapor deposition techniques was not conformal over high pyramids creating surface protrusions. Selective emitter was implemented by selective back etching using reactive ion etching technique in this step, which also removed the dead layer. RIE however causes surface damage; therefore an additional short time wet oxidation step was introduced to remove the surface damage. As a result efficiency improved to 13.1% from 11.2% with $FF$ improving to 73.5% from 62%. The IV characteristics of the champion cell are shown in figure 2.5. Simulation studies were also done to understand this result and to further improve the efficiency.

A solar cell process for n-type solar cell and front side boron emitter was developed. The process used spin-on-dopant and boric acid as dopant sources. N-type c-Si wafers, with <100> orientation and 1-5 Ω-cm resistivity, are chosen for the process. After RCA cleaning, wet oxidation process was done to achieve oxide layer of thickness of 200nm on both the sides of the wafer. The back surface oxide layer is removed to have N$^+$ doping with $P_2O_5$ solid source diffused at 975°C for 20min. Now the front surface oxide layer is removed and boric acid solution (2%) or B-SOD source is spun on and thereafter annealed at 200°C for 20 minutes. The drive-in is done at a temperature of 850°C for 10-20 minutes depending on the required sheet resistance values of the emitter. The whole diffusion process is optimized for sheet resistance values of 45-55 Ω/sq and 70-100 Ω/sq. In-situ oxidation (at 700°C, for 20 minutes), during ramping down, is used for reducing boron rich layer in case of B-SOD diffusion whereas no in-situ oxidation is required in case of boric acid diffusion as boron rich layer (BRL) formed here is comparatively thinner. Front surface is passivated with $Al_2O_3$ of thickness 70nm. In one set of solar cells aluminum is used as front contact and Ti/Pd/Ag is used as back contact and in other set of solar cells Ni-Cu electroplating is used for contact patterning. The resultant IV characteristics are shown in Fig. 2.6 and 2.7.
P type, CZ, <100>, 1-4 ohm –cm, 250 μ thick.

Boron (P+) Back Surface Field diffusion
Phosphorous (N+) front emitter diffusion

Mesa cell isolation by lithography
Etching leading to formation of selective emitters (N+/N)

Oxide/ Nitride bilayer ARC

Ti/Pd/Ag – front contact formation
Al back contact formation

The maximum efficiency obtained so far is on boric acid powder diffused 1cm² area solar cell with no passivating layer and for emitter sheet resistance value of 45Ω/sq. The details obtained for the cell are: $V_{oc} = 0.502$ V, $J_{sc} = 39.9$ mA/cm², FF= 27%, $R_s = 8.34$ mΩ, $R_{sh} = 13.92$ mΩ, efficiency = 5.39%. The cell suffers from high levels of shunting as can be appreciated from Fig. 2.6.

Unit Process Development:

1) **Texturing Process**: Two different texturization processes were developed during the year under review. Complete characterization of the texturization processes shown below are progressing.
   a) Plasma texturing of silicon surface: Plasma texturization process is an interesting process for multi crystal Si solar cells as the multi crystalline wafer has crystalline grains that are randomly oriented. This was tried out using SF$_6$ plasma in a reactive ion etching chamber. The areas having resist exhibited texturization, while resist free areas were not textured as can be seen in Fig. 2.8.
   b) Lithography free inverted texturing scheme: A novel lithography free inverted pyramidal texturing process using TMAH is also being investigated using silicon nitride as a mask. Silicon was etched through the blisters in SiNx:H formed as a consequence of annealing. The results are shown in Fig. 2.9. Inverted pyramids are seen in the figure. Further process development is required for uniform distribution of pyramids.
Fig. 2.8: SEM image of an inverted pyramid texturized Si (100) surface.

Fig. 2.9: SEM image of a random texturized Si (100) surface. Inverted pyramids are generated using a lithography-less technique.

2) Anti-reflective coating development:

The ARC layer developed in the previous year was extensively characterized for lifetime and thermal stability. It was seen that a hydrogen rich layer is required for passivation however this layer is susceptible to blistering upon annealing. A double layer is developed in which the layer interfacing the silicon surface is hydrogen rich and the second layer is poor in hydrogen. This combination is seen to provide the necessary ARC behaviour without blistering and high surface passivation. Fig. 2.10 shows the reflectance measured for a number of recipes with nitride thickness of ~ 70nm.

Fig. 2.10: Reflectance of polished c-Si surfaces coated with 70nm SiNx:H layers measured using UV-Vis spectrometer.

3) Optimization of Phosphorous Diffusion Processeses:

During the previous year, it was shown that an approximately 70 nm dead layer was formed after P-diffusion from a solid source. A wet etch process for removing this layer was developed. The composition of the etch solution was 10% HF:HNO₃:H₂O (1:60:6). Fig 2.11 shows the SIMS profiles before and after dead layer removal. The peak concentration has come down from $2 \times 10^{20} \text{cm}^{-3}$ to $3 \times 10^{19} \text{cm}^{-3}$ as a consequence of the deadlayer removal process. Fig. 2.12 shows the sheet resistance of junctions diffused at different temperatures before and after deadlayer removal. Diffusion at 900C was seen to provide the desired sheet resistance.
The formation of deadlayer as a function of diffusion temperature to probe whether a deadlayer removal step can be completely avoided. The resultant doping profiles are shown in Fig. 2.13. We see the emergence of a highly doped dead layer as the diffusion temperature is raised to 890 °C, from SIMS measurements. It is seen that a diffusion profile without deadlayer may be obtained for diffusion temperature in the range of 850°C. However the junction depth is in the range of 300nm for such low diffusion temperature. A selective emitter process was developed by etching out the deadlayer using reactive ion etching from select areas. The sheet resistance obtained as the etch time is varied is shown in Fig. 2.13. The area below contacts have 30 ohm/square and active area of the device have 90 ohm/square, optimized for low Auger recombination. The dead layer which is detrimental in effect is removed from the active layer of the device.

4) Optimization of Boron Diffusion for n-type solar cells:

Boron doping is optimized for the formation of emitters in the n-type solar cells and to act as a Back Surface Field in p-type solar cells. Formation of an impervious silicon boride (SiBₓ) layer was observed during Boron diffusion and a detailed structural analysis was carried out. TEM results (Fig. 2.15) show that the SiBₓ layer has island like morphology due to the clustering of the boron beyond critical concentration. A Low Temperature Oxidation (LTO) step with optimized temperature and time was introduced to remove this layer. The SIMS profile of boron with and without the LTO process are shown in Fig. 2.16. It is seen that the deadlayer is effective removed along with the low temperature oxide.
In another investigation, two limited boron dopant sources, boric acid powder and B-Spin on Dopant, were used for making the emitter of n-p junction. At diffusion temperature of 850°C, the emitter is optimized for 45-55 Ω/sq., and 70-95 Ω/sq. for various diffusion time. In-situ oxidation (at 700°C) during ramp down is very much essential to reduce the formation of boron rich layer (BRL) in B-SOD diffusion, which corroborated the observations stated in the previous paragraphs. Some unintended spot like structure cannot be avoided at the surface of the B-SOD diffused sample, but can be reduced when B-SOD source is mixed with Acetone in a ratio of B-SOD:Acetone = 4:1. In doing so, the sheet resistance value also increases to 90-125 Ω/sq from 45-55 Ω/sq. On the other hand, boric acid diffusion does not require any in-situ oxidation as BRL formed in this case is less compared to B-SOD. But the solution concentration is needed to be increased from 2% to 4% when the substrate size is increased from quarter of 2” wafer to complete 2” wafer for maintaining the same sheet resistance value of the emitter.

The interesting phenomenon seen in B-diffusion is that the unwanted BRL shows gettering effect. The minority carrier lifetime increases considerably in the presence of BRL and decreases when the layer is removed by some chemical treatment. Two chemical treatments- 1) HF (2%)- HNO₃ (conc., at 90°C)- HF (2% ) solution and 2) HNA (HF+HNO₃+Acetic acid) are used to remove BRL. The first one gives slightly lower value of minority carrier lifetime than that of BRL layer whereas HNA solution gives low lifetime value. So the second chemical treatment is discarded for removing BRL.

5) Surface passivation:

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Fig. 2.15: TEM images of the silicon surface showing SiBₓ layer.

Fig. 2.16: Boron profile with and without low temperature oxidation. LTO was etched prior to profiling.

Fig. 2.17: Surface recombination velocity as a function of post deposition anneal temperature for the best nitride recipe, R7. The inset shows the fixed dielectric charge and interface state density for various recipes.

Fig. 2.18: Cross section TEM image of AlOₓ deposited on Si by pulsed-DC sputtering process. An interfacial layer of 8nm thickness is seen between the Al₂O₃ and Si irrespective of the anneal conditions.
Thermally stable silicon nitride (SiN<sub>x</sub>:H) films were developed using an Inductively Coupled Plasma CVD system (ICP-CVD) for passivation of n-type Si surfaces. The reflectance results for these films are shown in Fig. 2.10. MOS capacitors were fabricated on p-type 4-7 ohm-cm <100> wafers with Al as the gate and substrate electrode. The interface state density and fixed oxide charge extracted form capacitance – voltage measurements are shown in the inset of Fig. 2.17. Effective minority carrier lifetime studies were carried out for the recipe 7 which showed the lowest interface state density. Optimized nitride films on n-type FZ wafers using a lifetime tester from Sinton Instruments. A minimum surface recombination velocity (SRV) of 1.9 cm/s was observed for the nitride on annealing it to 500°C for 2 secs after deposition as shown in Fig. 2.17. This temperature is compatible with Ni/Cu contacts used in high efficiency solar cells.

We have investigated Al2O3 deposited by pulsed-DC sputtering for passivation of p-type silicon surfaces. In the previous year it was shown that higher power of deposition results in a higher density of negative fixed charges in the film. The impact of post deposition anneal conditions were studied extensively during the year under review. TEM image of a typical sample is shown in Fig. 2.18. It is seen that the pulsed-DC sputtering process results in the formation of a interfacial layer which is approximately 8nm thick. The post deposition anneal is seen to have a significant impact on the passivation obtained. The best passivation is obtained for anneal in O<sub>2</sub> + N<sub>2</sub> ambient (dry air) at 520°C as seen in Fig. 2.19.

![Figure 2.19: Impact of post deposition anneal on (a) the negative fixed charge, (b) interface state density and (c) surface recombination velocity of Al2O3 deposited by pulsed-DC sputtering.](image-url)