12.2 Silicon Solar Cells

12.2.1. High Efficiency Crystalline Solar Cells

Fabrication of large area (5 inch X 5 inch) crystalline silicon solar cells (Dr. Saravanan and M. Rawal):

In this effort, solar cells on large area wafers are being processed. The first run wherein the wafers were subjected to texturization, and diffusion had to be stopped during the diffusion process due to POCl₃ leak. However the issue is being resolved and we expect to demonstrate large area cells in the near future. In the meanwhile we have obtained partly processed wafers from one of the IIAP partner of NCPRE and screen printing processes were tried on these wafers.

Process optimization of the front contact and back surface field for 5’ mono crystalline silicon wafers

- Front contact pattern has been designed in such a way to cover the 6-7% front side by having the grid line width of 80 micron and the bus bar of 1500 micron. And the screen parameters such as mesh count, emulsion thickness and tension were chosen in such a way to get the better aspect ratio in grid lines.
- Similarly the back surface field pattern has been designed by leaving 1 - 1.25 mm gap from the edges of the wafer so that shunting will be avoided
- The designs are shown in Figs 12.1

![Fig. 12.1. Front contact and back surface field designs.](image)

- By employing these designs with optimized printing parameters such as snap off, squeeze speed and pressure the front contact silver was printed. Printed cells were dried at 250 °C. The FC printed cell images are shown in Fig. 12.2. Paste weight was 130 milli grams
Further to front contact, back aluminum was printed and dried at 250 °C. The aluminum paste weight was about 1.05 gms

These cells were fired using rapid thermal process and the optimization of the temperature profile is in progress.

The consolidated Sun V_{oc} measurement on the trial cells are below

<table>
<thead>
<tr>
<th></th>
<th>V_{oc}(mV)</th>
<th>pFF(%)</th>
<th>Rsh(ohm-sq.cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trial 1</td>
<td>548</td>
<td>82.925</td>
<td>4890.25</td>
</tr>
<tr>
<td>Trial 2</td>
<td>520</td>
<td>81.525</td>
<td>41681.75</td>
</tr>
</tbody>
</table>

Monocrystalline silicon solar cells on n-type substrates (Bandana Singha):

Optimization of output characteristics of solar cells with boron spin on dopnat (BSOD) diffusion at temperature 850°C for 10mins and post oxidation at 700°C for 20mins was done for V_{oc} values in between 470-490mV and I_{sc} values in the range 37- 39.8mA/cm². The efficiency values of the cell were in the range 9-10%. These cells did not have any texturization or passivation.

Present study is basically to enhance the efficiency by texturing and passivation.

Experiment done:

- KOH/ IPA texturing has been optimized for pyramidal height 4-6µm and TMAH texturing has been optimized for pyramidal height 300- 800nm.
- Emitter sheet resistance values were optimized for diffusion at 850°C for 10mins

Future work:

- Fabrication of solar cells with textured surface
Texturing (Mallikarjunachari):

Using NaOH and IPA, an average reflectance of 12% was obtained during the previous quarter. In this quarter we have tried to further optimize the process to reduce average reflectance. The cross section SEM images of the wafers subjected to typical texturization process are shown in Fig. 12.3. Reflectance plots for various texturization conditions are shown in Fig. 12.4. Texturization was done at 80°C for 20 minutes in all the cases.

![SEM images of textured samples by NaOH (2.5 wt %) solution with different IPA concentration](image1)

![Reflectance curves of samples textured by NaOH solution with different IPA concentration.](image2)

![Average reflectance as a function of the concentrations of NaOH and IPA. The reflectance is averaged over 400 nm to 1100 nm.](image3)

Of the various recipes attempted, 2.5 wt% NaOH with 6 wt% IPA is seen to result in the lowest average reflectance.

Al₂O₃ deposited by reactive sputtering for surface passivation (Meenakshi Bhaisare)
In the previous quarter we had reported the passivation of p-Si surface using pulsed DC sputter deposited Aluminum Oxide and the thermal stability of the passivation. During the quarter under review, we have carried out physical analysis of the films to gain further understanding of the passivation mechanism.

Cross-sectional transmission electron micrograms (TEM) of the film on silicon is shown on Fig. 12.6. The measurements are carried out for as-deposited and annealed AlO$_x$ film at 520 °C in N$_2$ + O$_2$ gas mixer (79: 21) for 20 min, which has given the lowest $S_{eff}$ of ~ 41 cm.s$^{-1}$. These films contain high negative fixed oxide charge density ($Q_f$) ~ $6 \times 10^{12}$ cm$^{-2}$ and low interface state densities ($D_{it}$) ~ $4.3 \times 10^{11}$ eV$^{-1}$ cm$^{-2}$.

From the contrast we observe that the films can be divided into two regions, an interfacial layer (IL) between Si and AlO$_x$ with thickness ~ 8.2 nm and an AlO$_x$ layer with thickness of 21.4 nm and 19.9 nm for the as-deposited and after annealed films, respectively. Although a small change in the thickness of the AlO$_x$ is seen after annealing, this is within the process control in our experiment and it cannot be attributed to any systematic changes with annealing. Thus no significant dependence of annealing condition is observed on the thickness of the IL or AlO$_x$ layer. The IL is relatively thick for p-DC reactive sputtered AlO$_x$ films for both as-deposited and annealed conditions compared to AlO$_x$ deposited by ALD. The surface passivation quality observed is much better for annealed AlO$_x$ films as compared to as-deposited films. Since the thickness of IL is not affecting the passivation quality for these films, the composition of films is analyzed using depth resolved XPS measurement for clearer understanding.

![Fig. 12.6](image)

**Fig. 12.6:** Cross sectional TEM images of AlO$_x$ film deposited on c-Si (a) as-deposited film, and (b) annealed film in N$_2$ + O$_2$ gas mixer at 520 °C for 20 min.
Fig. 12.7: Atomic concentration profile of AlO$_x$ film after PDA in N$_2$ + O$_2$ ambient at 520 °C using XPS measurements.

Fig. 12.7 shows the depth profile of various elements in AlO$_x$ film obtained using XPS analysis, for samples annealed in N$_2$ + O$_2$ ambient at 520 °C for 20 min. Atomic concentration is plotted as a function of etch time. The films shows 60 atomic % of oxygen and 40 atomic % Al near the top surface, which indicates that the film near the surface is stoichiometric Al$_2$O$_3$ with O: Al ratio of 1.5. However below this stoichiometric layer, the atomic concentrations of O and Al are almost equal and so O: Al ratio is 1. Further deeper into the film, it is observed that the Al concentration decreases and the silicon concentration increases gradually, whereas the oxygen concentration remains constant. In the IL region, the peak related to SiO is also seen in the XPS data. The IL is aluminum silicate for the process described here. The film is stoichiometric Al$_2$O$_3$ close to the surface, and this is most likely due to the re-oxidation of the surface during the annealing ambient used here. However for as-deposited films we observed the O: Al ratio is ~ 1 throughout the AlO$_x$ region, figure is not shown here. In comparison to ALD films, the interfacial layer thickness is relatively high (~ 2nm for ALD versus 8nm for sputtering). There are reports that the passivation quality decreases with the thickness of the interfacial layer. Subsequent process optimization efforts would target thinner IL.

Low Temperature Oxy-nitride for Surface Passivation of Silicon Solar Cells (Sandeep S S)

During the previous quarter we had reported on a low temperature oxide growth process using plasma. In the quarter under review, we have further optimized the process. Plasma Oxides were grown in an Inductively Coupled Plasma chamber and were studied for its surface passivation properties. The films were grown in Oxygen, Oxygen – Argon mixture, Oxygen – Nitrogen mixture and Nitrous Oxide ambient at 320°C. The plasma characteristics were studied using an Optical Emission Spectrograph (OES). These thin oxide films were capped with Silicon nitride (SiN$_x$::H) deposited using an Inductively Coupled Plasma CVD system (ICP-CVD). MOS capacitors were fabricated on p-type 4-7 ohm-cm <100> wafers with Al as the gate and substrate electrode. Effective minority carrier lifetime studies were carried out for optimized nitride films on n-type FZ wafers using a lifetime tester from Sinton Instruments.
The optical emission spectra (OES) for various plasmas used are shown in Fig. 12.8. OES revealed two major atomic lines of oxygen at 777nm and 844nm corresponding to the atomic transitions $3p^5P - 3s^3S$ and $3p^3P - 3s^3S$ respectively. When Argon was introduced, the intensity of the oxygen related peaks remained same. On adding nitrogen, the intensity of the peak at 777nm remained same, while the intensity of the peak at 844nm decreased. For nitrous oxide plasma, both the 777nm, and 844nm peaks came down in magnitude indicating lesser amount of oxygen radicals. FTIR data for oxides grown in different plasmas are shown in Fig. 12.9. The Si-O-Si stretching mode trough is seen to shift from 1100cm$^{-1}$ to 1060cm$^{-1}$ on addition of argon or nitrogen. For the samples grown in oxygen ambient, a prominent peak at 510cm$^{-1}$ can be seen, which corresponds to SiO$_4$ bending mode vibrations. Addition of Argon results in decrease in the concentration of SiO$_4$ bonds while a trough indicating Si-Si unsaturated bonds at 615cm$^{-1}$ is seen to form. For samples grown in O$_2$+N$_2$ ambient, the trough at 510cm$^{-1}$ is absent, while a deeper trough at 610cm$^{-1}$is observed. For samples grown in N$_2$O ambient, there are no troughs seen at 510cm$^{-1}$ or 615cm$^{-1}$.

The interface property of the Si-dielectric interface was investigated using MOS capacitors. The interface state density ($D_{it}$) was measured from the conductance – voltage curve using the single frequency approximation method, while the fixed oxide charge ($Q_{ox}$) was measured from the shift in mid-gap voltage. The usage of an interfacial oxy-nitride film thus improves the passivation of the silicon surface. Fig 12.10 shows the variation of the lifetime with minority carrier density. For the as grown samples, it was observed that the $D_{it}$ was in excess of $10^{12}$ev$^{-1}$cm$^{-2}$. On capping these films with a SiN$_x$:H layer, $D_{it}$ in the range of 5 - 7x$10^{11}$ev$^{-1}$cm$^{-2}$ for samples grown in O$_2$, O$_2$+N$_2$ and O$_2$+Ar ambient. For samples grown in N$_2$O ambient, the $D_{it}$ was found to be a1.6x$10^{11}$ev$^{-1}$cm$^{-2}$.

Surface passivation studies were carried out on the various stacks and it was found that the stack based on N$_2$O based plasma oxide resulted in the lowest surface recombination velocity (SRV), while the stack based on O$_2$ plasma resulted in the highest SRV, as can be seen in Fig. 12.11. The SRV decreased for all samples upon annealing at 400°C, with the stack based on N$_2$O showing a minimum SRV of 50cm/s at a minority carried density of $10^{15}$cm$^{-3}$. SRV calculations have assumed an infinite bulk lifetime for the FZ wafer.
Contact grid optimization (Karthick Murukesan):

Contact resistance plays important role in the fill factor of solar cells. In our previous attempts of TLM measurements the measured resistance were inconsistent and at different points along the same contact pad varying resistances were measured. The problem was identified and eliminated by introducing a additional step during the fabrication of the sample. The sample preparation process involves 2 level lithography and the corresponding designed masks as shown in the Fig. 12.12 and Fig. 12.13 were used. The contact grid as in Fig. 12.12 has a finger with width of 90 micron. The least spacing between the contacts is 100 micron, which is then increased in terms of geometric progression for each device dice. The square dices as in figure 2b are of 2cm, 1cm and 0.5 cm size. The device dices are boron doped to form P/N junctions. They are subsequently contacted by evaporated Al.

Before this process of contact formation the sample has been subjected to ashing in oxygen plasma to remove any residual ppr and subsequently it has been given a BHF (5:1) dip just before the deposition to remove any native oxide formed. After this additional step being introduced the problem of inconsistent resistance values along the contact finger has been eliminated. The results and further observations are as follows.

A representative 4 probe measurements done over 0.5cm square dice is shown in Fig. 12.14.
Parameters obtained from the graph are $R_c=0.198$, $L_t=135$ micron, Contact resistivity $=10.4E^{-4}$ ohm-cm$^2$. Sheet resistance extracted from slope of the fitted line – 100 ohm/square. The measured sheet resistance by four probe measurement is 80-85 ohm per square. The resistance corresponding to the 1600 micron separation doesn’t fit with the other resistance measurements in the linear fit and varies largely. The only experimental parameter to check the effectiveness of this technique and reliability of the extracted values is the sheet resistance which is also slightly varying. To figure this out several other changes are planned in the measurement methodology and mask design which will be reported in further reports.

12.2.2. 3D Junctions (Student: Som Mondal)

Salient features:
The objective of this activity is to fabricate vertical junctions using Laser Annealing. The current research direction in this work is to estimate the junction depth using HF/HNO$_3$ solution due to differential etch mechanism in p and n-type surface.

Detailed progress report:
The junction depths were estimated using the stain etching method in this case. The etchant solution contains HF:HNO$_3$:H$_2$O in a ratio of 100:1:50. Before the etching the solution was activated with a heavily doped p-type sample. Samples were etched in the solution for 10 min and then thoroughly rinsed in DI water.

Fig. 12.15 depicts the morphology of the Phosphorous diffused surface after different etching time. The initial incubation time for reaction was observed to be varying from 1 – 3 min.
Once the reaction started, NO bubble emission was observed. These bubbles restrict the propagation of reaction and hence should be removed by adding some surface active chemical. After 5 min of etching the surface becomes sufficiently coarse to look stained. If the etching is continued further, the emitter gets etched out completely and the p-type substrate gets exposed. Fig. 12.15a presents the surface morphology after 5 min of etching. As time of etching increases, the evolution of bubbles slows down. After 45 – 50 min, the bubble formation was observed to be very slow. The surface becomes highly defective after 60 min of etching (Fig. 12.15b). Etching for 120 min is sufficient to remove the emitter. The surface morphology in Fig. 12.15c, thus, represents the surface of p-type substrate.

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Fig. 12.15: Surface morphology of the Phosphorous diffused surface in p-type substrate after (a) 5 min, (b) 60 min and (c) 120 min.

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Fig. 12.16 shows junction depth measured for different scan speed of laser using this technique. The laser beam has a very shallow depth of focus. Hence the repeatability of these results depends on the precise positioning of the focal plane on the sample surface. Significant variation of junction depth is obtained for samples prepared with same scan speed. However it is apparently observed that with higher speed during laser doping the junction depth reduces. The values presented in Fig. 12.16 are the maximum value obtained for each scan speed. Fig. 12.17 shows the cross-sectional SEM of the sample scanned with a speed of 20 mm/s. The selective emitter region looks coarse as compared to substrate. The separation of diffused region and substrate is clearly visible. The junction depth measured is 2.9 µm. The selective emitter formed after laser doping remains continuous with emitter as shown in Fig. 12.17. The average depth of emitter was measured to be 419 nm. As the etchant solution attacks the surface from both front and cross-sectional surface, the actual junction depth may be higher than measured value. The surfaces coarsening with long etching time may be attributed to the destructive etching as reported by Winton et al (1997). The difference in etch rate between p-type and n-type surface is also visible from microscopic images. However, staining is also observed sometimes on laser irradiated p-type substrate (without doping source). This may be attributed to higher activity of HNO₃ in defects generated by laser irradiation. Further work is being carried out to identify such defect formation and etching behavior at such locations.
12.2.3. Novel technology for contact formation using temperature sensitive paste (Sastry)

Objective:
To open ARC selectively using chemical etching paste in finger- bus bar grid pattern. The finger width should be less than 100 µm and should process industrial solar cells.

Salient features:
To reduce the finger width of c-Si solar cell metallization at front (preferably less than 100 µm). Should be applicable for industry process.

Detailed Experimental work:
To remove ARC, chemical etching method by electro-discharge machine (EDM) wire is performed on half-finished solar cells. Finger opening width of 47 µm was achieved using a 30 µm EDM wires and 87 µm was achieved using a 50 µm EDM wires. Opened finger using EDM wire is shown in the fig. 12.20 at a width 102 µm.
Since the EDM wire patterning manual method has limitations in continuity and finer finger widths, the experimental procedure is slightly modified. The experiment is conducted on a 3d-stage. Using 50 µm EDM wires, variation range started from 70-200 µm (opening of a finger) and 50-150 in the case of 30 µm wire with the 3d-stage. These are the previous results from 3d stage experiments. With these results, the finger variation obtained is very high. To optimize uniform finger width, it is necessary to reduce the variation of finger width along a single finger.

**Fig. 12.19: 3d stage and cell holder.**

**Fig. 12.20: Measurement of a finger width, 102 µm after etching.**

**Observations:**
The EDM wire is fixed to an acrylic sheet which is in C-shape and again fixed to the stage. In this case, the acrylic sheet will move along with the stage in vertical direction (up and down) once to catch the paste and finally to print on the solar cell. Since the paste applied on the wire is not uniform, which causes large variations on the printed lines. This is confirmed with the cross section images of paste printed solar cells.

One possible way to avoid the excess amount of paste which is being transferred to the cell from wire is to remove it. A small slit (more than wire thickness ~ 100 µm) can help in removing the excess amount of paste as well as improve uniformity. To incorporate slit to the current design, moving of the slit will be a problem with ~ 100 µm. Any small variation can create impact on printed line on solar cell. Better solution for this could be a moving wire. In the current design, rotating wheels will support the wire to pass and circulate.
Using the rotating discs, the wire is rotated with the help of a motor. Once the wire comes down, it is subjected to enter through a small slit. The slit has bigger inlet and smaller outlet. After it comes out of the slit, it is subjected to move down to the solar cell. Using this design, uniformity can be achieved. This is shown in the fig. 12.21. Currently the design is under progress.

Simulation:
- To estimate exact amount of paste required
- To evaluate the contact angle between paste and the wire surface.

The simulation is under progress for the contact angle between paste and the wire surface.

12.2.5 Ni/Cu metallization for front contact (Mehul Raval)

**Salient Features:** Ni seed layer deposition in range of 50-100nm from alkaline bath with characterization of contact resistivity ($\rho_c$) and silicide phase.

**Experimental Conditions and characterization:**
Electroless Ni alkaline bath was used for Ni deposition. Typically for an alkaline bath, a high bath temperature is required and hence bath temperature was maintained in the range of 90-95°C. Plating time intervals were in the range of 30-45s to obtain thickness in the range of 50-100nm. Constant bath pH was maintained during the experiments by addition of ammonium hydroxide (NH$_4$OH). Temperature and pH were constantly monitored during the plating process.

For silicide formation, samples with 50nm and 100nm Ni seed layer were annealed at 500°C and 550°C for 30s respectively. Contact Resistivity measurements were done using the conventional TLM approach. Current of 20 mA was maintained during the measurements. A set of 3 to 5 samples were fabricated for each specific annealing condition. For determination of silicide phase, the unreacted Ni was etched in an H$_2$SO$_4$: H$_2$O$_2$ (1:1) solution after annealing. The phase was then determined using XPS technique.

**Results and Discussions:**
Fig. 12.22 shows the Ni seed layer growth for a deposition time of 30s. It can be observed that the thickness is in the range of 30-50nm and the particle growth seems to be progressing in the interval range. A more uniform seed layer of thickness close to 105nm is obtained for plating interval of 45s as indicated in fig. 12.23.

From TLM measurements, ρ values in the range of 1 to 2.3mΩ-cm² were measured for Ni seed layer of 100nm. These values are close to the requirement of 2mΩ-cm² for solar cell metallization. XPS data for the two seed layers annealed at respective conditions are shown in table 2. It can be inferred that for both seed layer, the phase of nickel silicide was Ni₂Si. Since the desired phase is NiSi, the annealing conditions need to be tuned to achieve the same.

<table>
<thead>
<tr>
<th>Ni thickness (nm)</th>
<th>Annealing conditions (°C,s)</th>
<th>XPS Peaks</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Ni2p</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Obtained(eV)</td>
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<tr>
<td>50</td>
<td>500,30</td>
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<tr>
<td>100</td>
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<td>852.7</td>
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Ni-Cu Front side Metallization of c-Si solar cells and its adhesion problem (Vishnu Kant Bajpai):

Salient features:
The Ni/Cu front-contact metallization scheme for c-Si solar cells is a low cost and potentially useful for high efficiency solar cells manufacturing.

Objective
The objective is to improve the adhesion of contacts without any performance sacrifice.

Experimental results and discussions
Mainly the experiments were performed to study and improve the nickel film deposition using electroless chemical bath deposition. Electroless Ni deposition is optimized and qualitatively significant improvement has been observed in adhesion of the Ni-Cu contacts.
with silicon. Now on applying mechanical stresses to the solar cell even up to the breakage of cell, the contacts do not peel off.

Fig. 12.24: SEM image of ~100 nm uniform Ni deposition on textured front side of the Si solar cell.

Fig. 12.25: Optical image of ~ 48 μm thick Cu-electroplated contact on textured front side of the Si solar cell with better adhesion.

Fig. 12.26: Variation of aspect ratio with respect to plating period and Cu-electroplated thickness at current density of 5 mA/cm² and keeping rest of the parameters constant.

It is found that the key process in the nickel-copper deposition process is the nickel seed layer formation. Because successive processes (like: silicide formation at the Ni-Si interface, Cu-electroplating etc.) are very much dependent on it and in turn adhesion and solar cell performance vary a lot.
Additionally a study is carried out for getting high aspect ratio front contacts using direct laser patterning. It is found that fine line patterning has very significant effect over aspect ratio. By reducing the finger width and using optimized process, beyond 0.5 of the value of aspect ratio can be achieved.

**Plasmonics for Photovoltaic Application (Hemant Kumar Singh)**

**Experimental Investigation of Plasmonic Effect:**
As in the previous report, we had mentioned about the nanoparticles surface coverage tuning using ultrasonication method. As we have said that the ultrasonication method is able to reduce the surface coverage of Ag NPs which resulted in reduced reflection compared to un-ultrasonicated samples in visible region, however this reduction in Ag NPs from surface affect the plasmonic behaviour at longer wavelength. To explore more about this, SEM is done for these samples [OLS -2 (Si/SiNx(80nm)/AgNP(15s))] SEM image analysis indicates (Fig. 12.28) that there is a trade off between surface coverage and inter-particle distribution as though the surface coverage decreases the reflectance in visible region decreases but at higher wavelength it seems to be increasing.

It can be seen from table 3 that the ultrsonication of such samples reduces the particle coverage but not at large extent as still the total reflectance high is as high as ~ 17%. Which suggest that the particle adhesion with surface is very good and ultrasonication is not as very good option for surface coverage tuning and also it indicates that and we need to look for alternative technique where we can control the surface coverage as well as inter-particle distribution and for that, the work is in progress.

![Fig. 12.27: Total reflectance vs incident wavelength plot for Ag NP based samples before and after ultrasonication.](image)

![Table 3: Calculated weighted total reflectance for OLS -2 (Si/SiNx(80nm)/AgNP(15s)) samples.](table)

Further, as we annealed the Mo thin film to form Mo nanoparticles by annealing method, however the SEM images indicates that the Mo film after annealing is not forming very good nanoparticles as silver does, rather it forms some zig-zag structure as shown in the fig. 12.29. Though optically it shows that there is no drastic impact on the sample reflection profile but after annealing it increases the reflectance and it is increased throughout as shown in fig. 12.29. Here MoNP indicates the Mo film which was annealed. It suggest that the Mo thin film are better than zig-zag shaped Mo particles.
12.2.6 Slicing of silicon wafers for PV applications using Wire Electric Discharge Machining (We-EDM) (G. Dongre, Kamesh Joshi, Gaurav Sharma)

Experimental work in minimization of kerf width:
The experimental analysis shows the kerf width generated by the wire-EDM process is using 50 μm by using 40 μm diameter wire. This is much smaller than the kerf width of abrasive wire saw process (200-250 μm) with 180 μm diameter steel wire and SiC abrasives of 5-30 μm. The comparative evaluation of kerf width generated in abrasive wire saw and wire-EDM process is given in Fig. 12.30.
The minimum wire size in abrasive wire saw is 180 μm, whereas in wire-EDM process wire up to size of 40 μm can be used to slice 3” silicon ingot. The Fig. 12.31 shows photographs of the kerf width achieved by using various diameter molybdenum wires. As shown in a graphical analysis in Fig. 12.31(e), the kerf width for abrasive wire saw process is 250 μm, whereas kerf width in a wire-EDM process depends upon the wire diameter. It can be reduced to 50 μm by using 40 μm molybdenum wire, which gives 200-300 % reduction in the kerf loss.
In this experimental study, slicing of 3” silicon ingot has been carried out by using 40 μm diameter molybdenum wire. However, 6” silicon ingot has been sliced by using 80 μm wire. The Fig. 12.32 shows the kerf width generated using 40 μm wire during silicon ingot slicing by wire-EDM process.

**Experimentation on thin wafer slicing**

A series of experiments was performed based on a certain combination of process parameters to produce minimum possible wafer thickness. The cut samples were analyzed using 3-D Optical Profiler for surface roughness. Fig. 12.33 shows the wafer thickness comparison between the existing and the proposed method of the silicon ingot slicing. The wires used for slicing are molybdenum wires having diameters within the range of 40 to 120 μm and minimum potential wafer thickness achieved is 120 μm for 3” silicon wafer using 60 μm wire, it is the lowest wafer thickness possible by a wire-EDM process. However, it is possible to slice 6” silicon ingot with minimum wafer thickness of 200 μm using 100 μm molybdenum wire. This wafer thickness is very much lower than the existing minimum wafer thickness achieved by an abrasive wire-saw process, i.e. 250 μm after etching and polishing. Past literature study has shown that the 100 μm wafer thickness will give maximum power conversion efficiency for PV application.
Concluding remarks:
The use of wire-EDM technology for slicing of silicon ingots reduces kerf width from 250 μm that is obtained during traditional abrasive saw cutting methods, to 50 μm, giving net material saving of 200-300%. The wire-EDM process for silicon ingot slicing improves surface roughness from 3-5 μm to 2-3 μm and overall improvement in productivity by 40% have been demonstrated over and above the conventional methods of silicon ingot slicing. At the same time, the process is capable of producing very thin wafers of size 100-125 μm thick which after etching and polishing can reach to the size less than 100 μm. It is demonstrated that the wire-EDM technology has the potential to produce ultra-thin silicon wafers with minimum kerf loss.