Potential induced degradation and light induced degradation in c-Si solar cells

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Outline

- IV measurement of solar cells
- Potential induced degradation (PID)
  - What is it?
  - Basic mechanism
  - Recovery
  - Mitigation strategies
  - PID test standard
- Light induced degradation (LID)
  - What is it?
  - Basic mechanism
  - Mitigation strategies

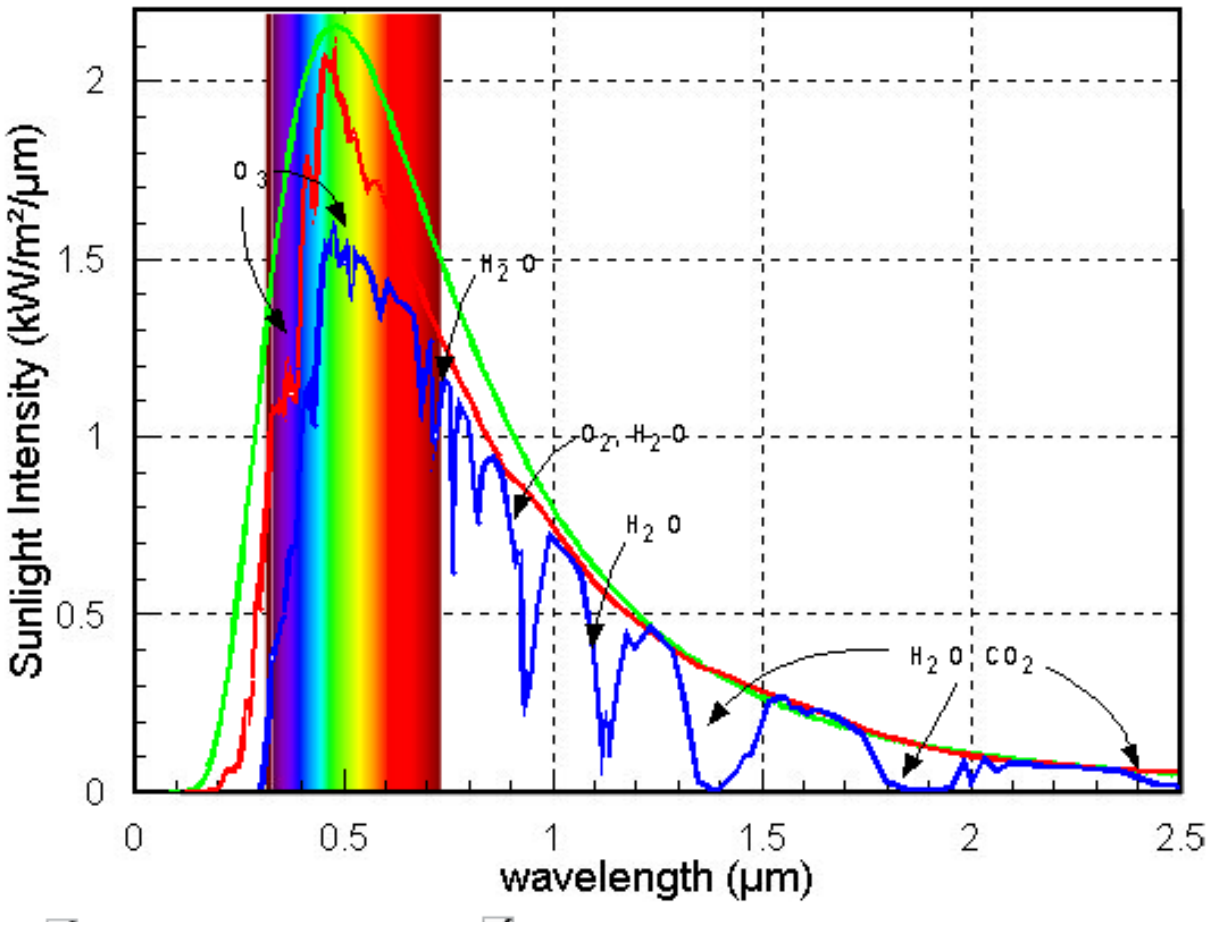
IV measurement of solar cells

STC:

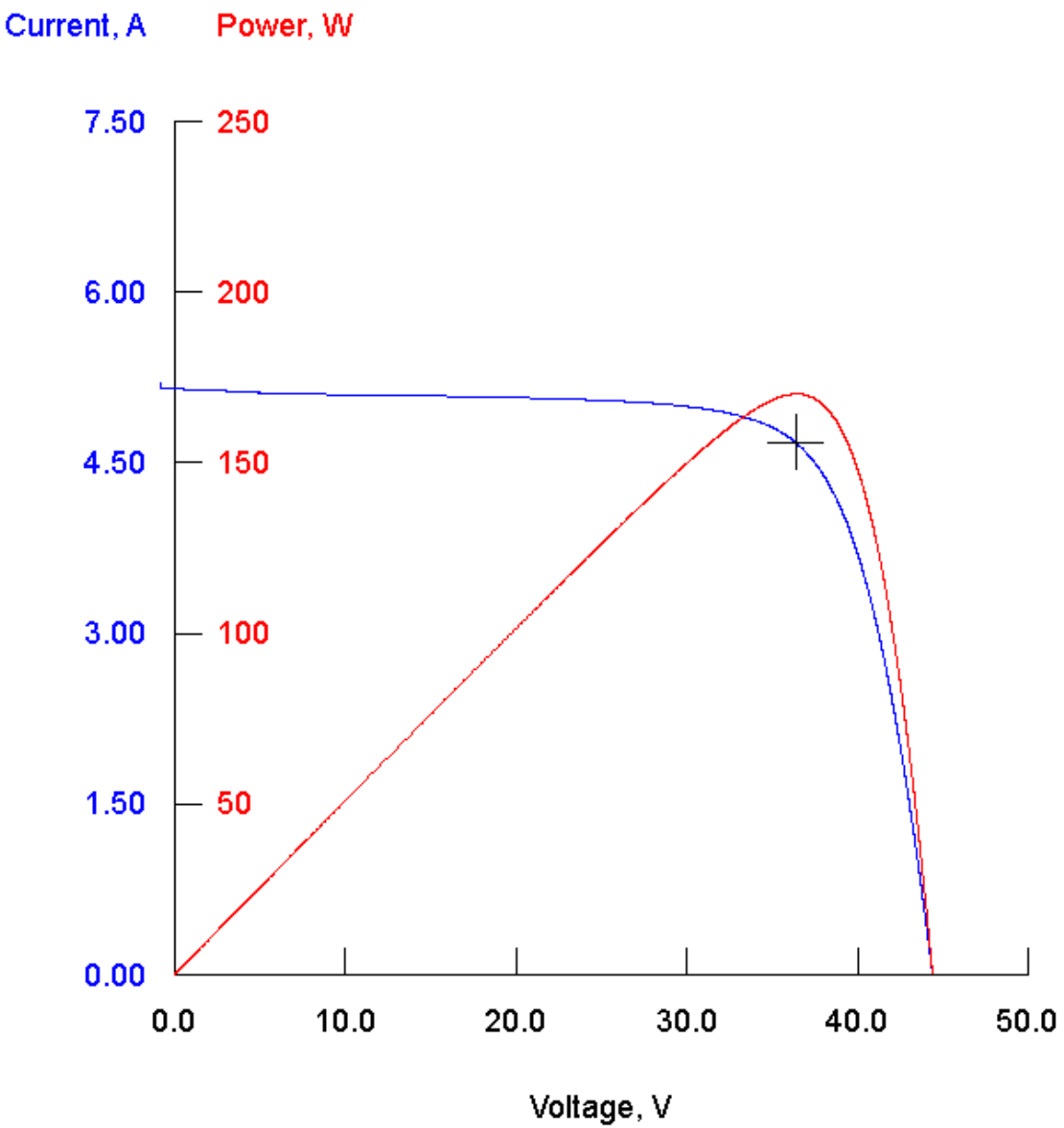
AM1.5

Temperature of 25°C

Irradiance: 1000 W/m^2

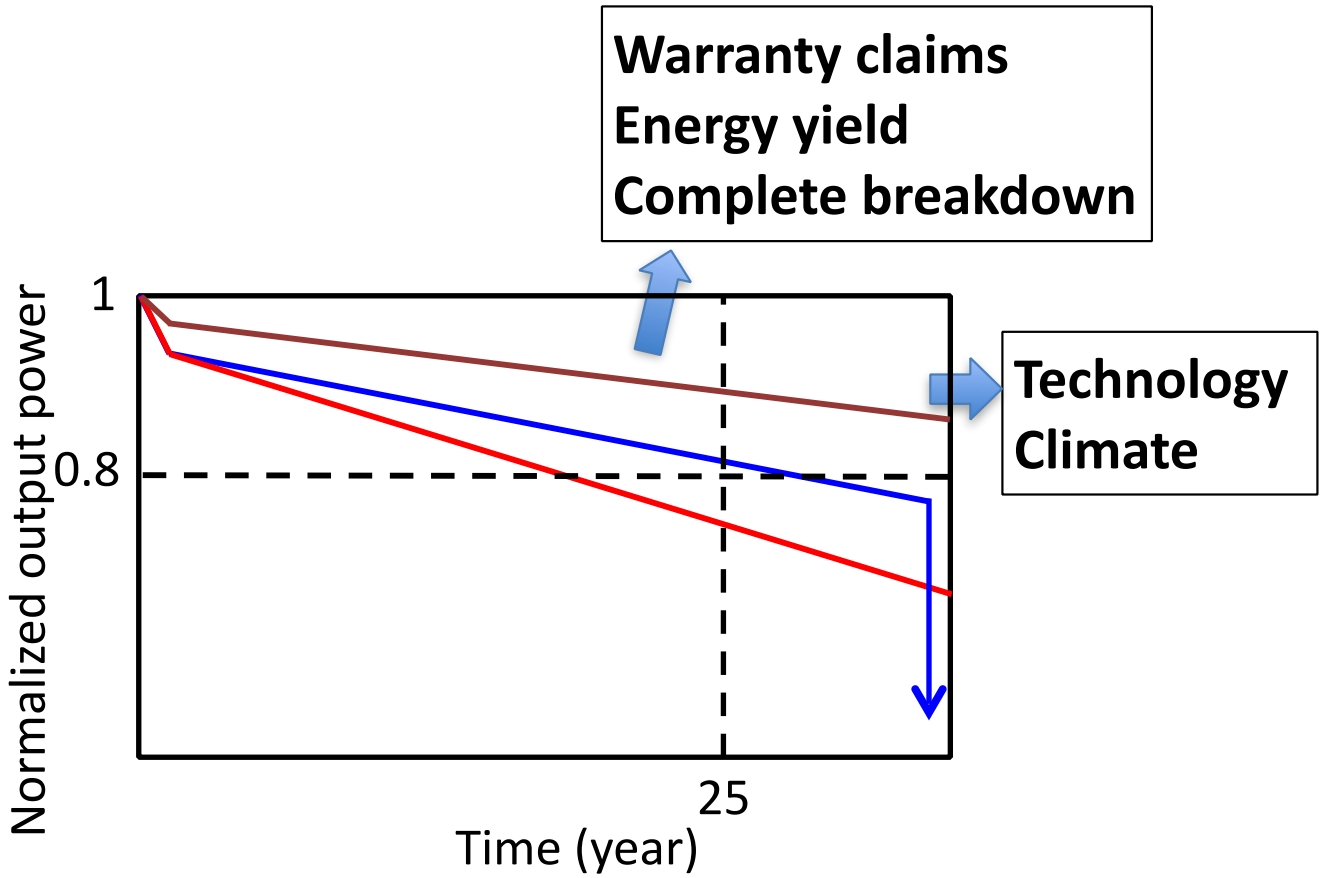


IV measurement of solar cells



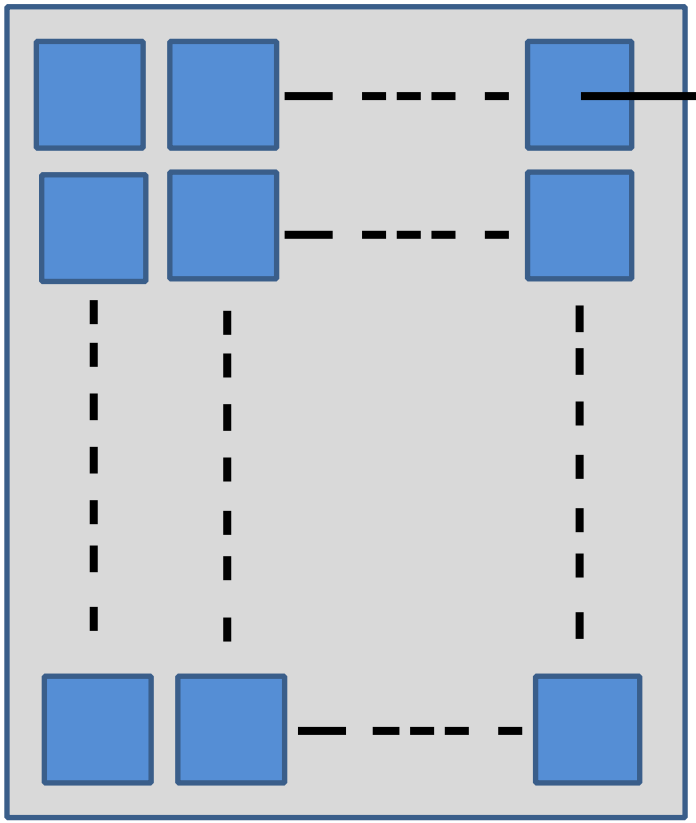
Measured Temp:	25.3 °C
Corrected Temp:	25.0 °C
Irr Meas:	99.9mW/cm²
Irr Corr:	100.0mW/cm²
Voc:	44.398V
Isc:	5.146A
Pmax:	170.129W
Vpm:	36.411V
Ipm:	4.673A
FF:	0.745
Eff,c:	15.901%
Eff,m:	13.350%
Rs:	0.857 Ohm
Rsh:	177.865 Ohm
MCCC1:	0.968
MCCC2:	0.963
Intensity V:	5.835V
Capacitor Voltage:	2240V
Load V:	7.180V
Sampling Frequency:	240000 Hz
Sweep Delay:	10 ms
Sweep Length:	70 ms
Sweep Direction:	Isc->Voc
IV Points:	2757

Implications of on-field degradation



NCPRE/NISE; All-India Survey of Photovoltaic Module Degradation:2013

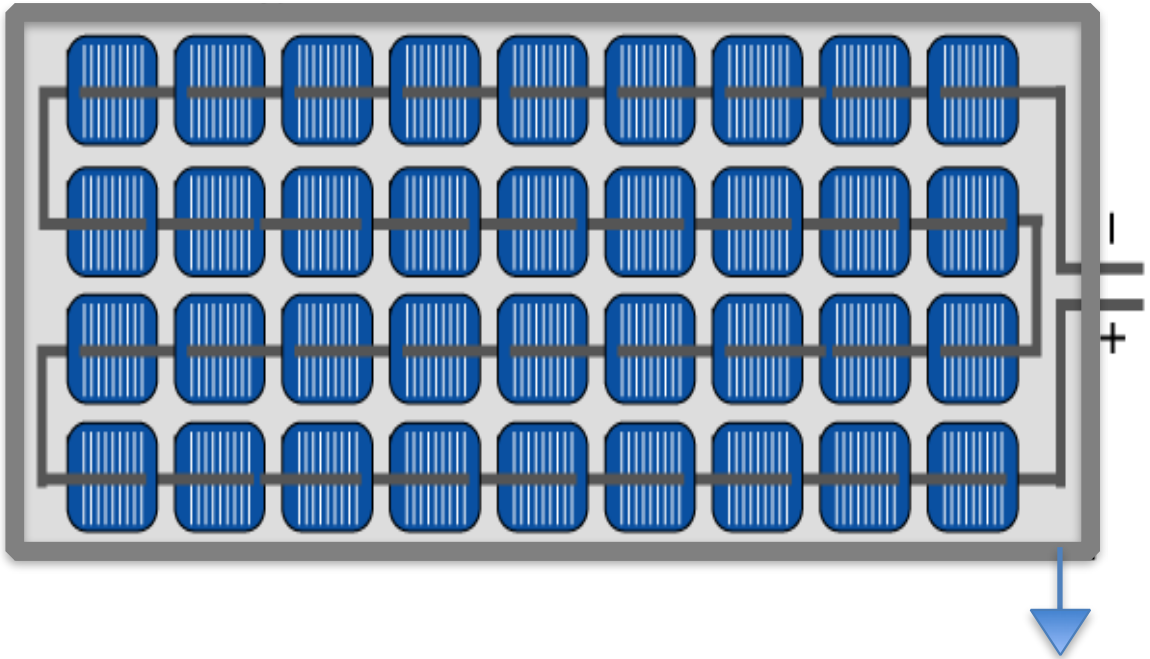
What is PID?

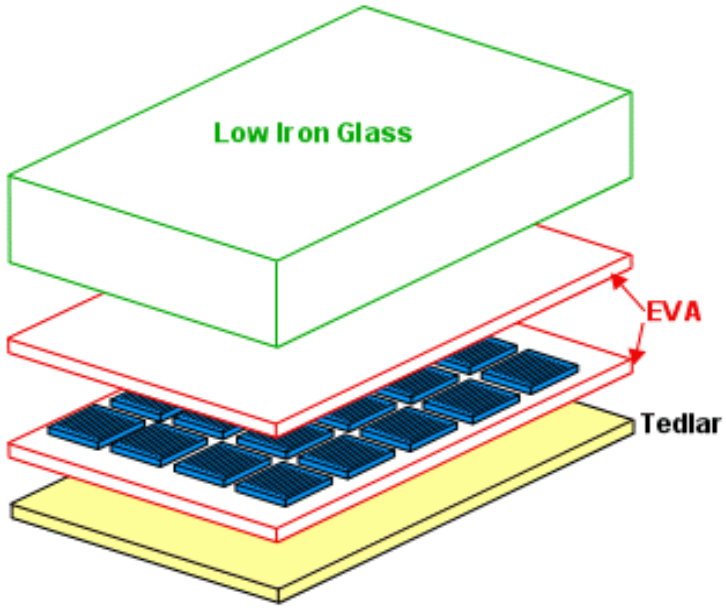


Solar PV installation

PV Module

What is PID? (2)

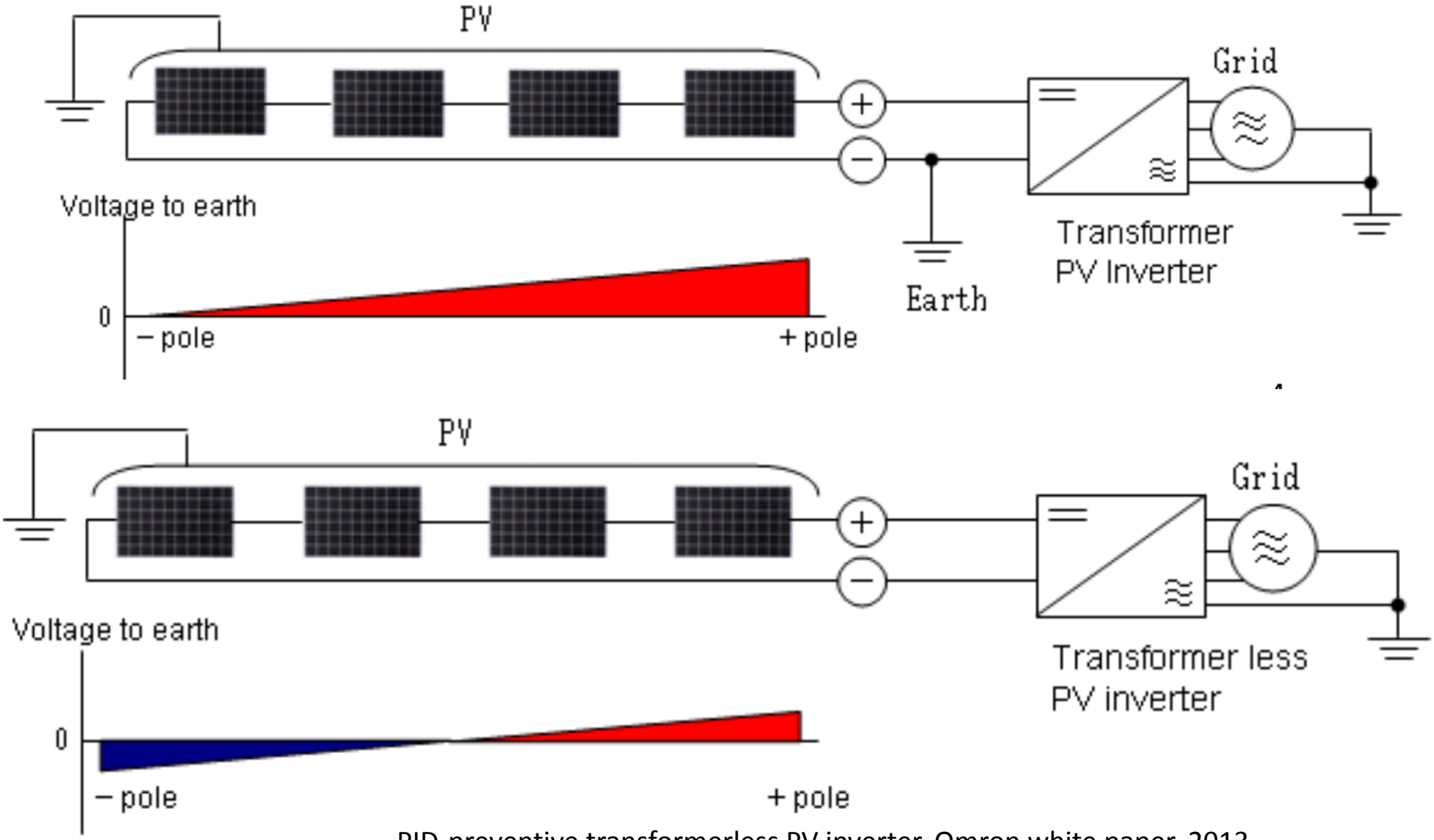




Important components of a module:

- Front glass – Solda lime glass
- Encapsulant – Ethyl Vinyl Acetate (EVA)
- Solar cells
- Backsheet - Tedlar
- Frame – Aluminum

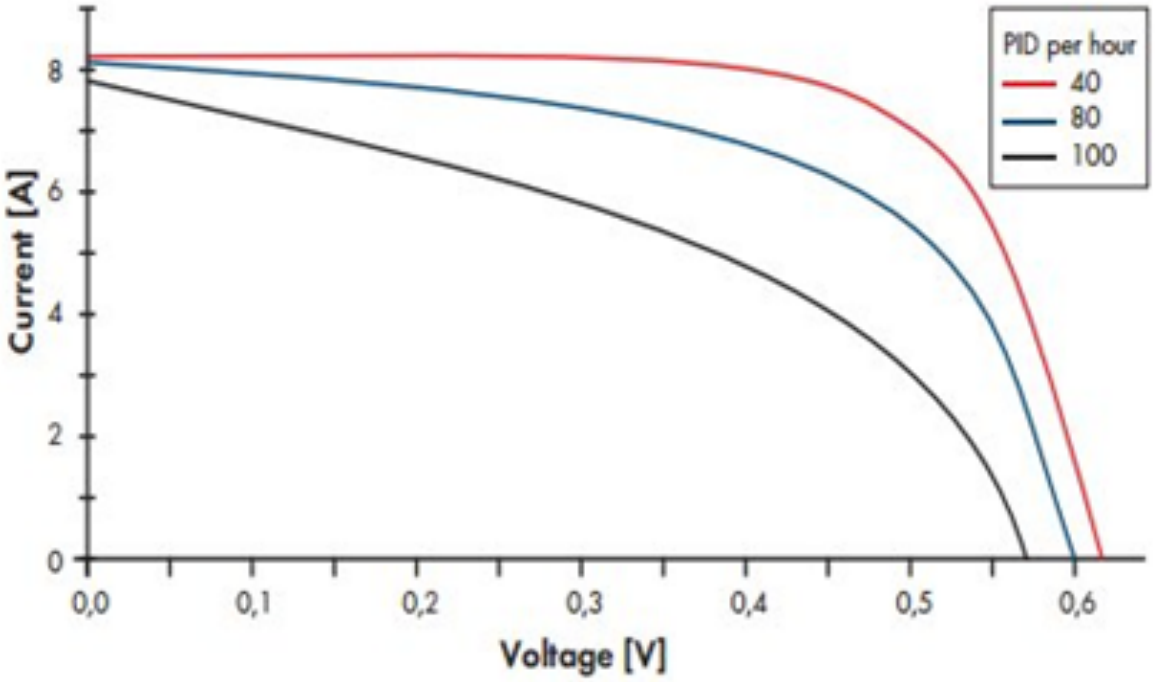
What is PID? (3)



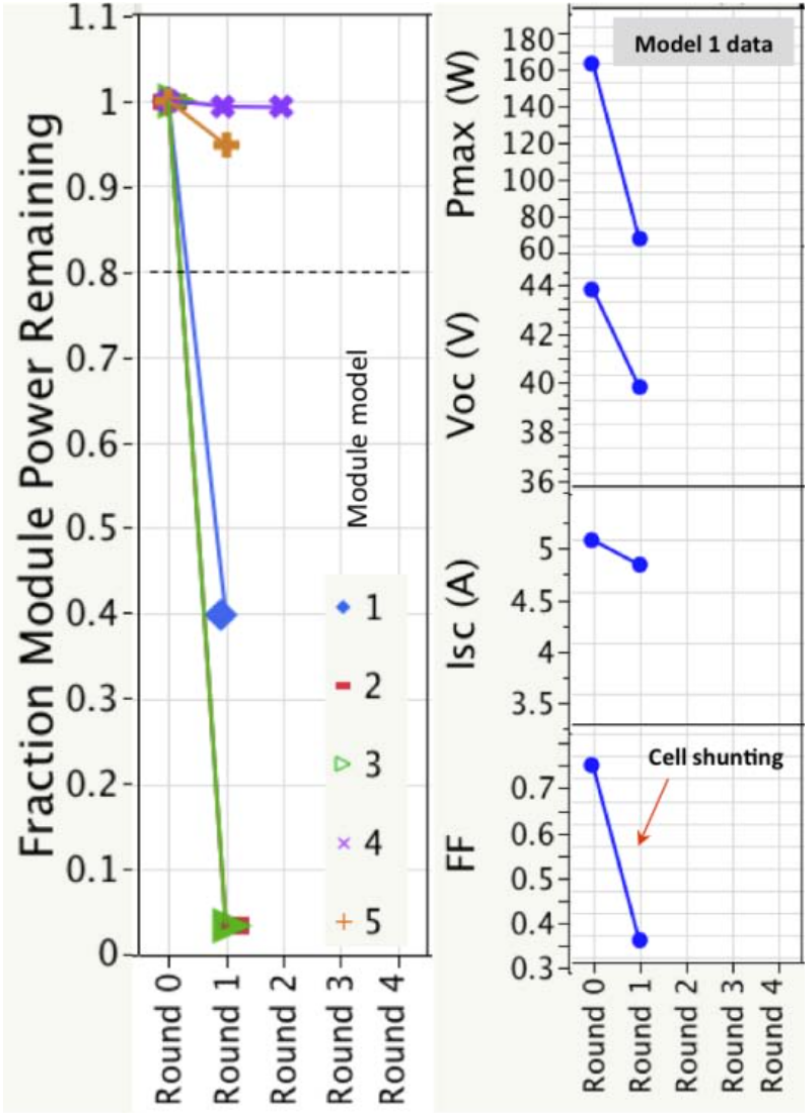
PID-preventive transformerless PV inverter, Omron white paper, 2013

What is PID? (4)

When modules are at the negative end of the string.

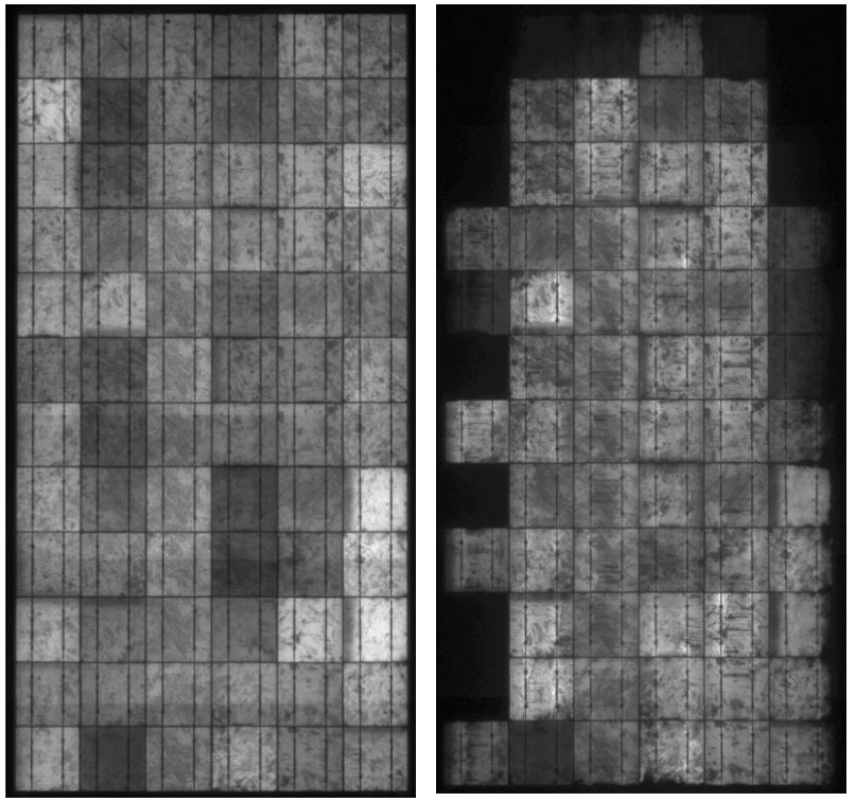


www.cenergymaxpower.com

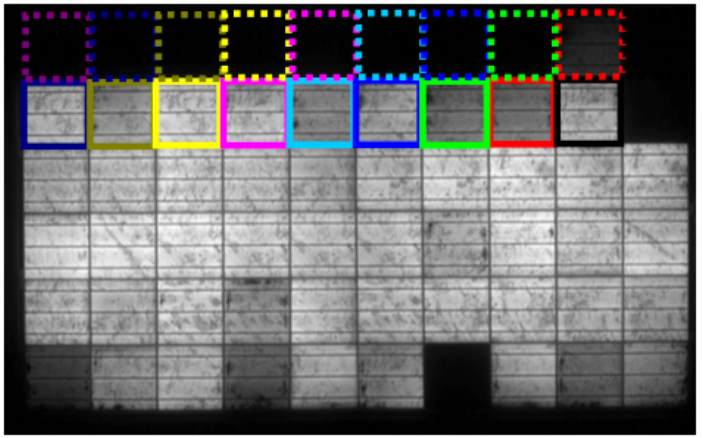


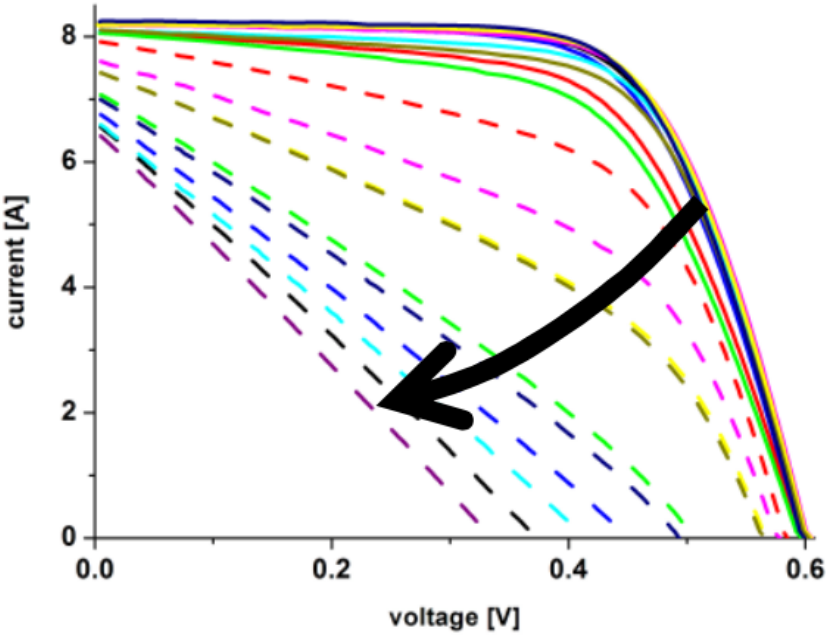
Hacke et al., EU PVSEC 2010

What is PID? (5)



Hacke et al., NREL, 2014

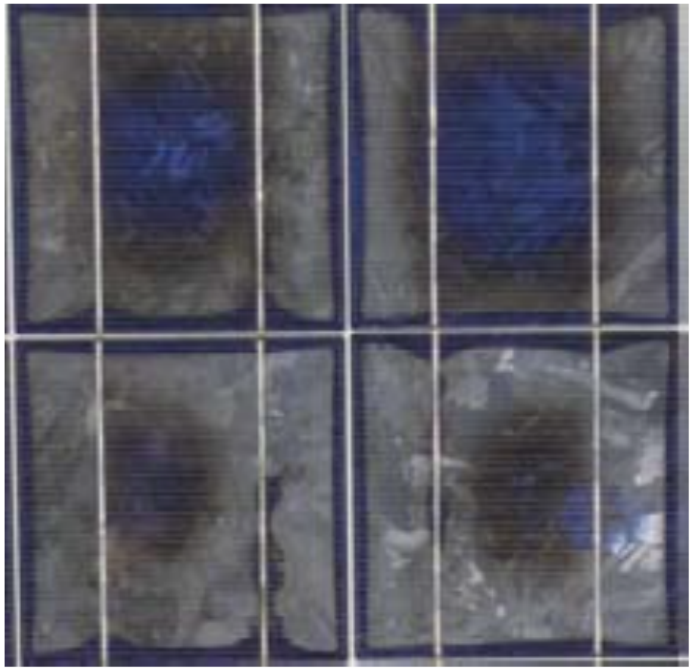




Schuetze et al., IEEE PVSC 2011

PID is nonuniform across the module

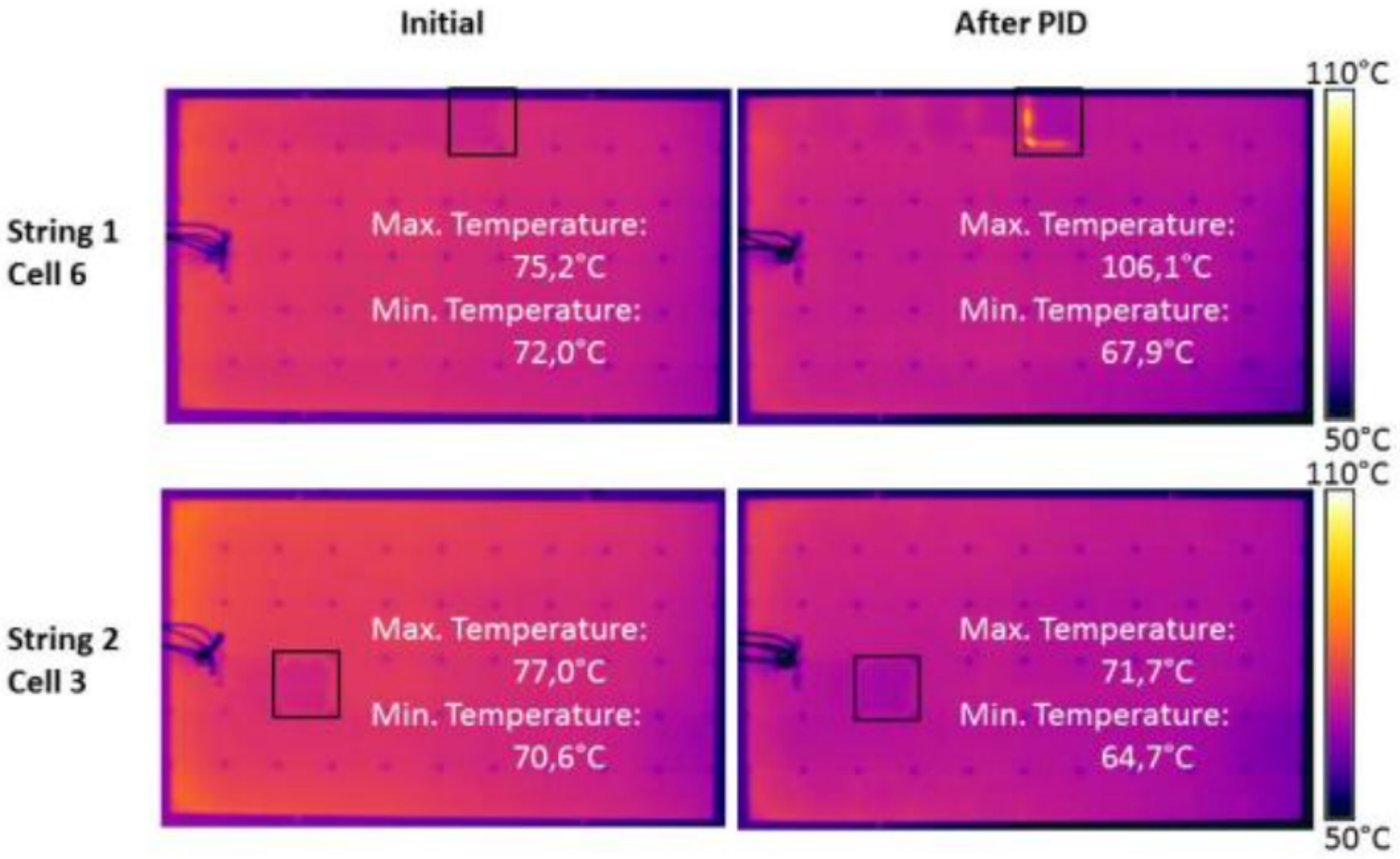
What is PID?



Silicon nitride is seen to be etched from the cells due to PID.
-600 V, 85C/85% RH, 1000 hrs.

Hacke et al., EU PVSEC 2010

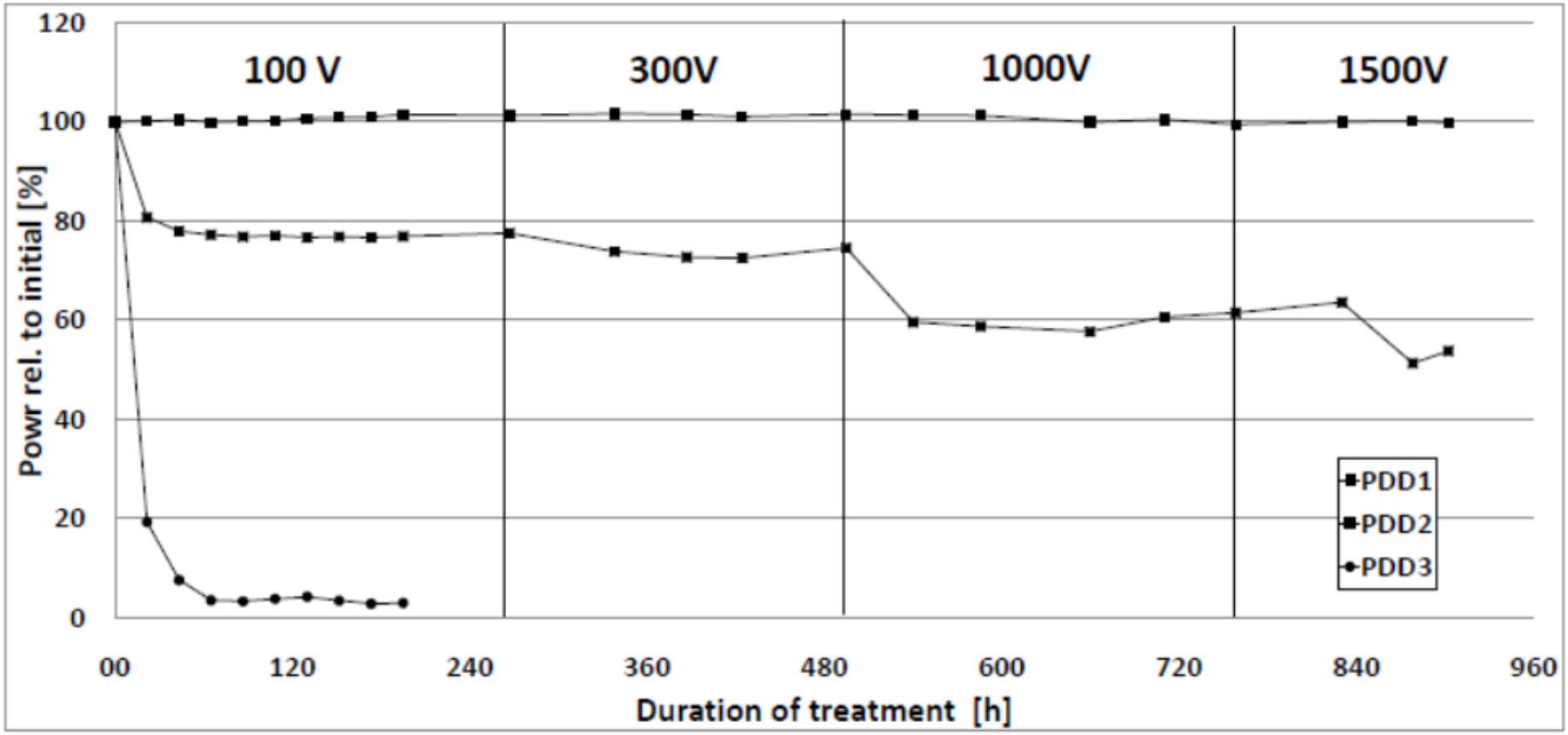
PID and hot spot



PID prone module

Koch et al., EU PVSEC 2012

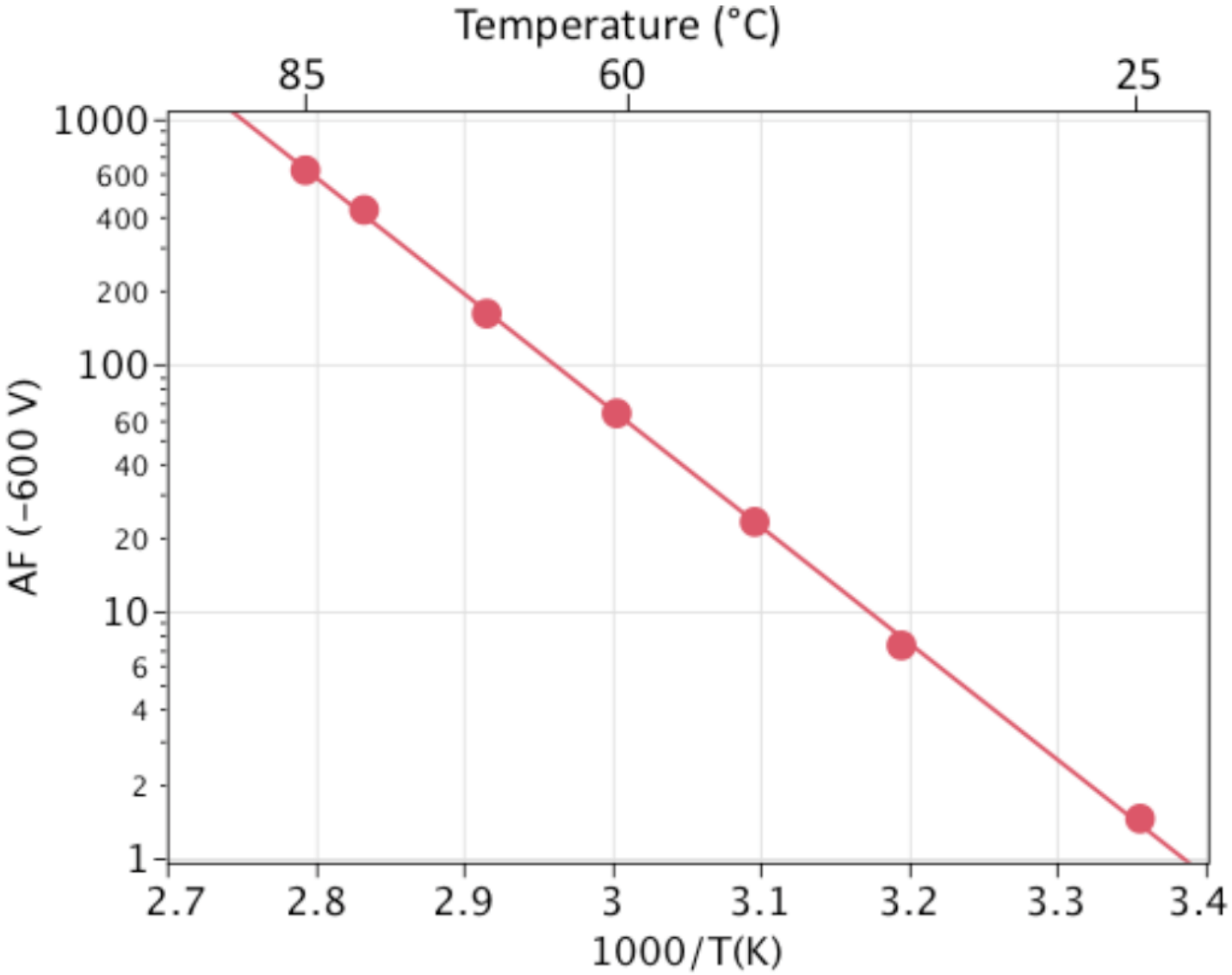
Impact of voltage



- PDDX – different module technologies
- All voltages are negative on the cells

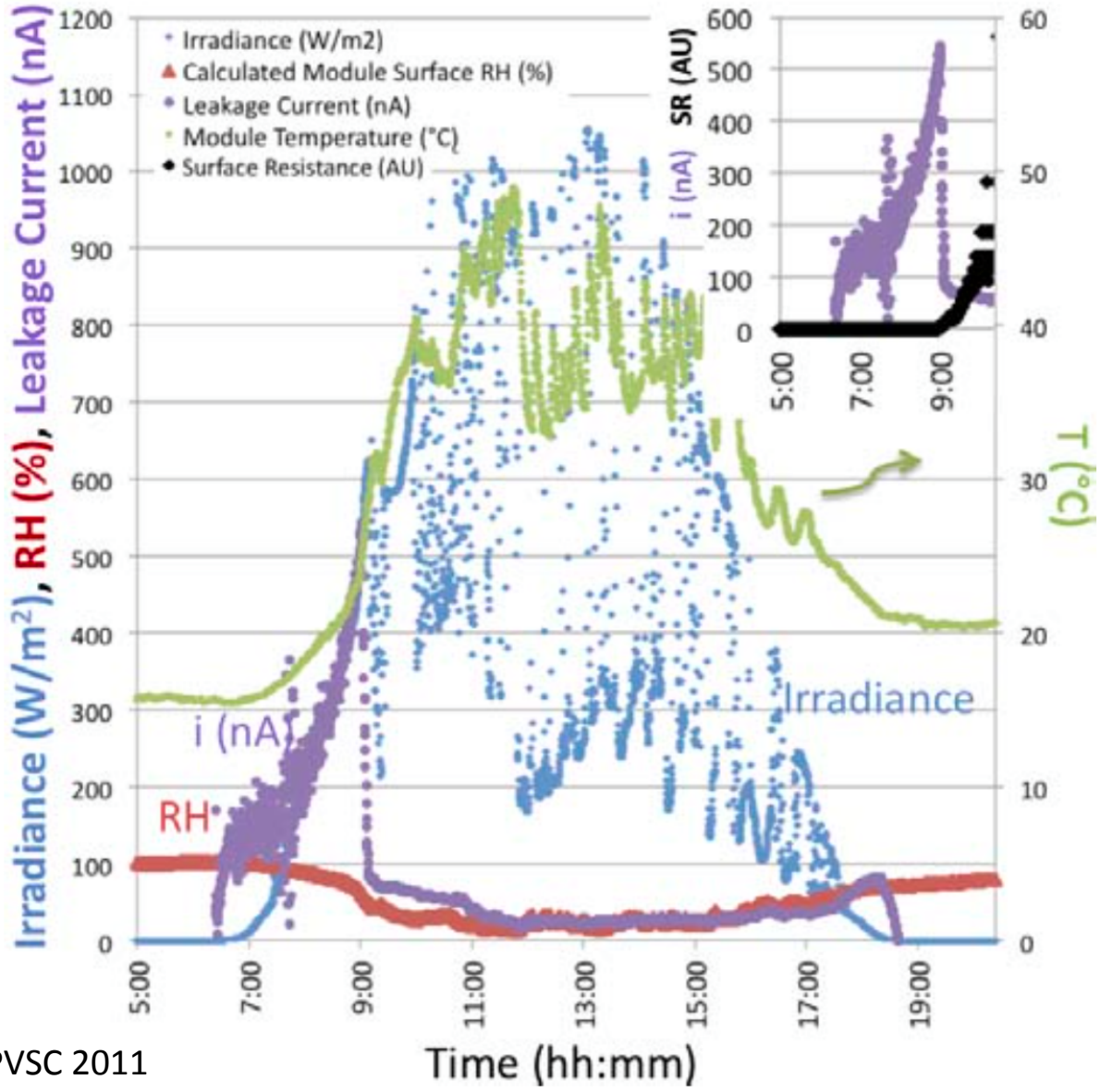
Koch et al., EU PVSEC 2011

Impact of temperature



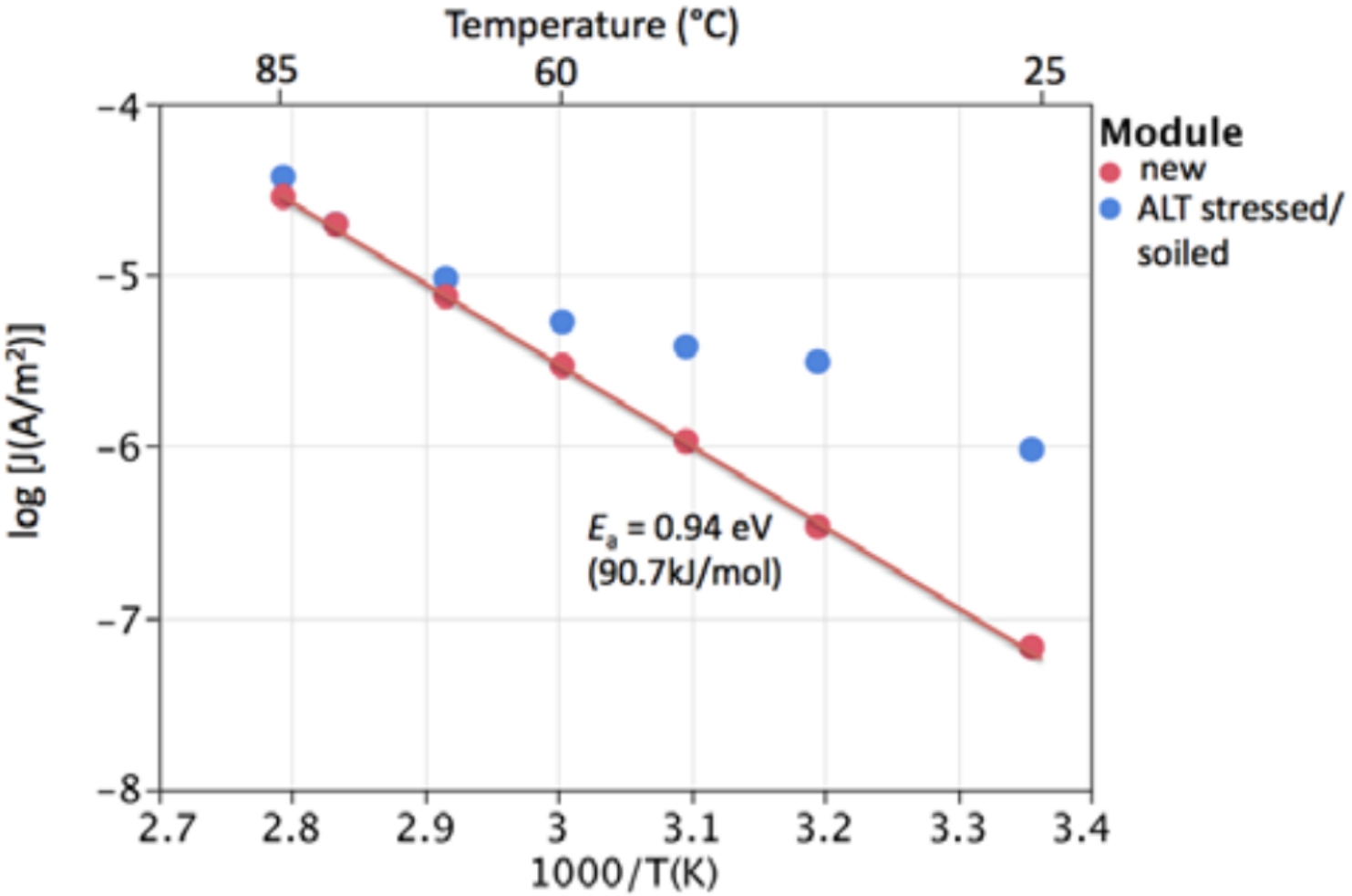
Hacke et al., IEEE PVSC 2011

Impact of humidity



Hacke et al., IEEE PVSC 2011

Impact of dust



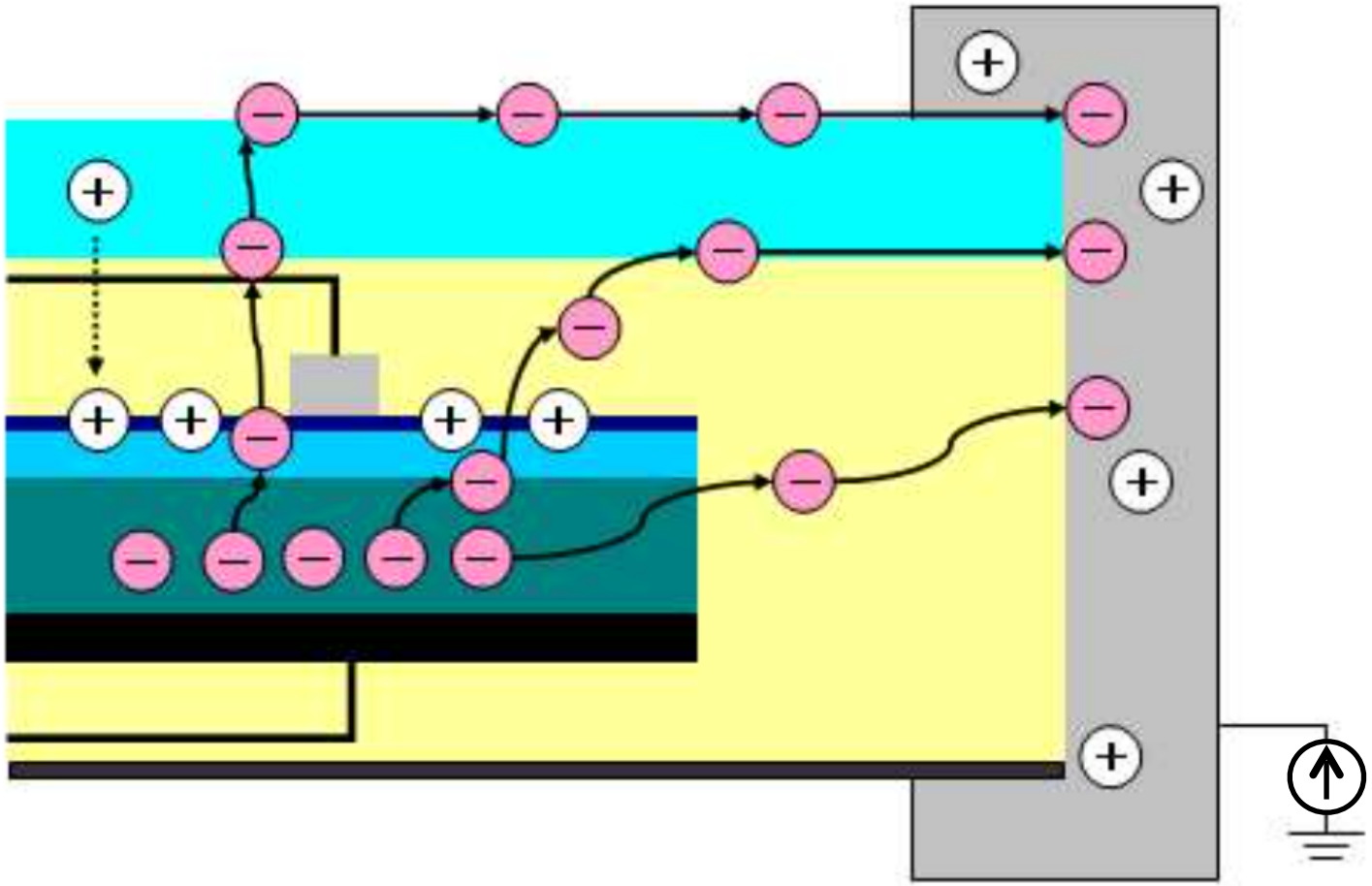
Hacke et al., IEEE PVSC 2011

PID - observations

- Large power loss is seen in modules when they are at the negative end of strings
- The major component of loss is the FF loss, due to creation of shunts in the solar cells.
- Electroluminescence (EL) is a powerful tool to diagnose PID. NCPRE proposed day-light EL could be deployed in field for this.
- Degradation is nonuniform across the module, and is seen to be more severe near the frame.
- Degradation is accelerated by voltage, temperature, humidity and dust.

PID mechanism

Cell is at negative potential



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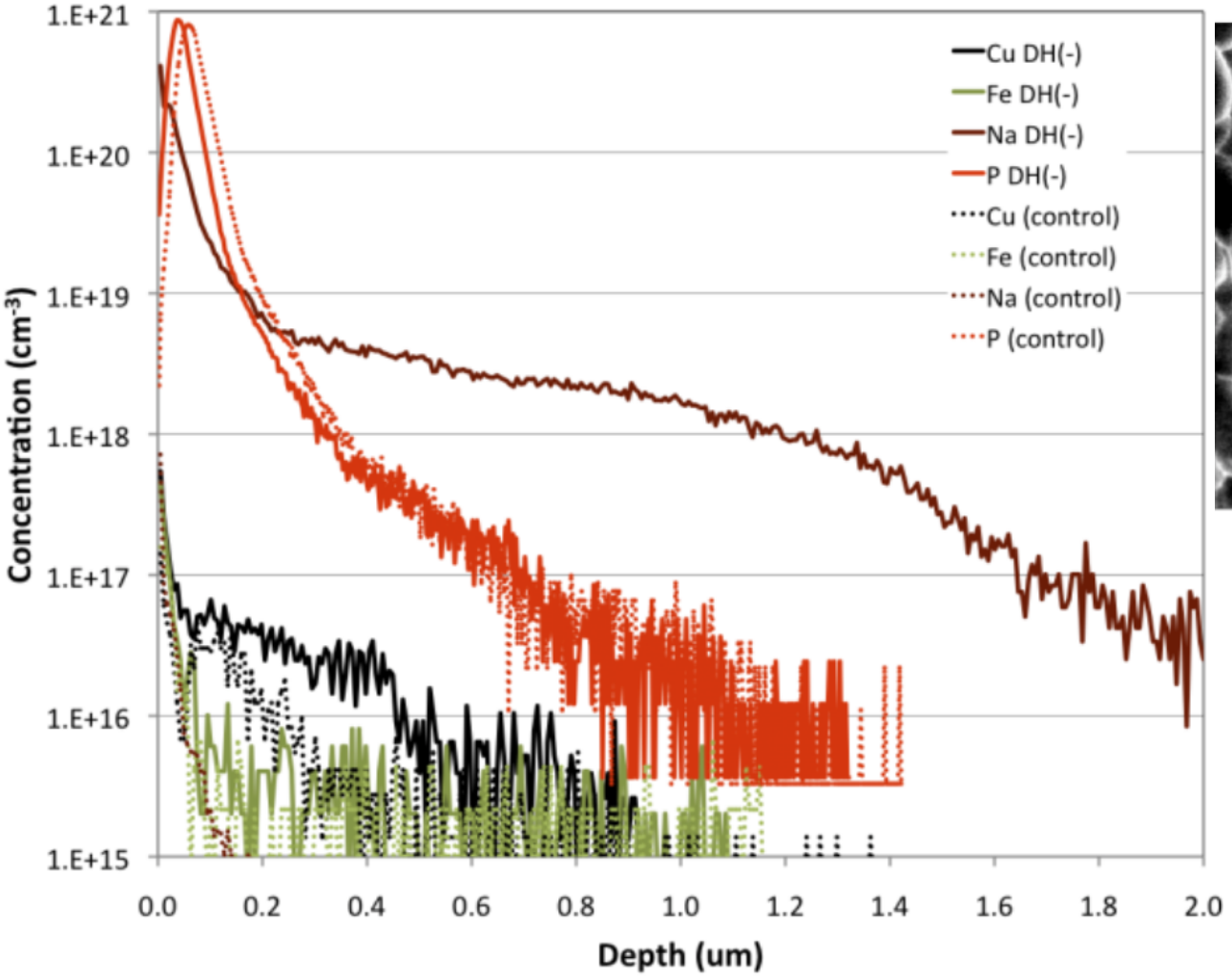
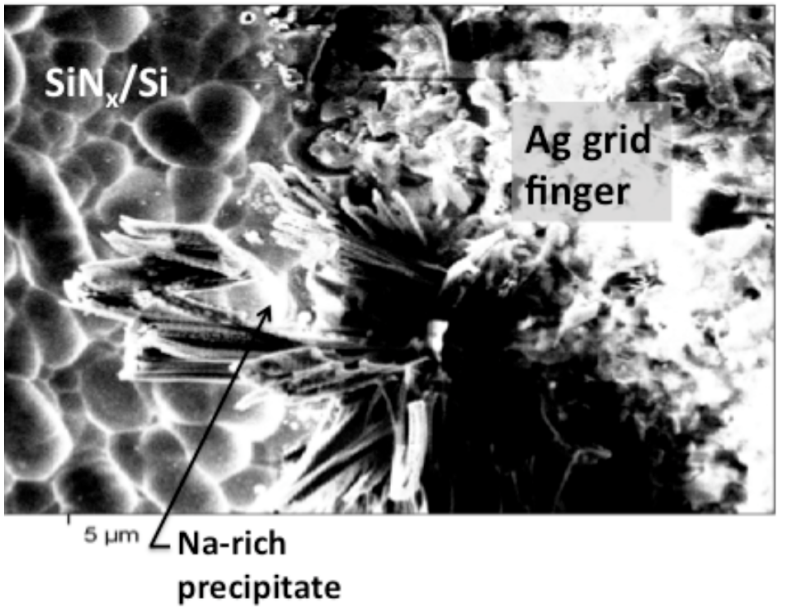
PID mechanism – role of sodium



Hacke et al., EU PVSEC 2010



Hacke et al., IEEE PVSC 2011

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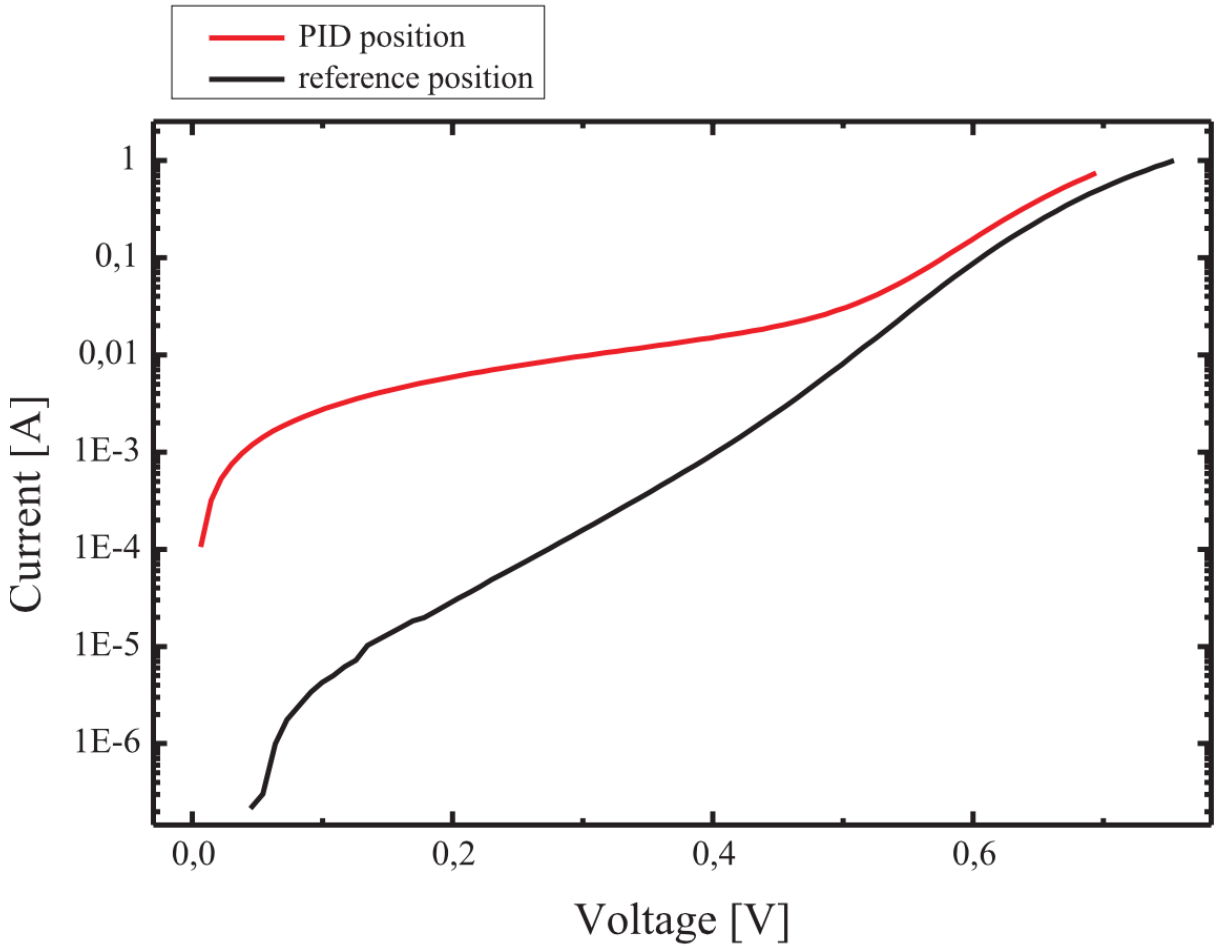
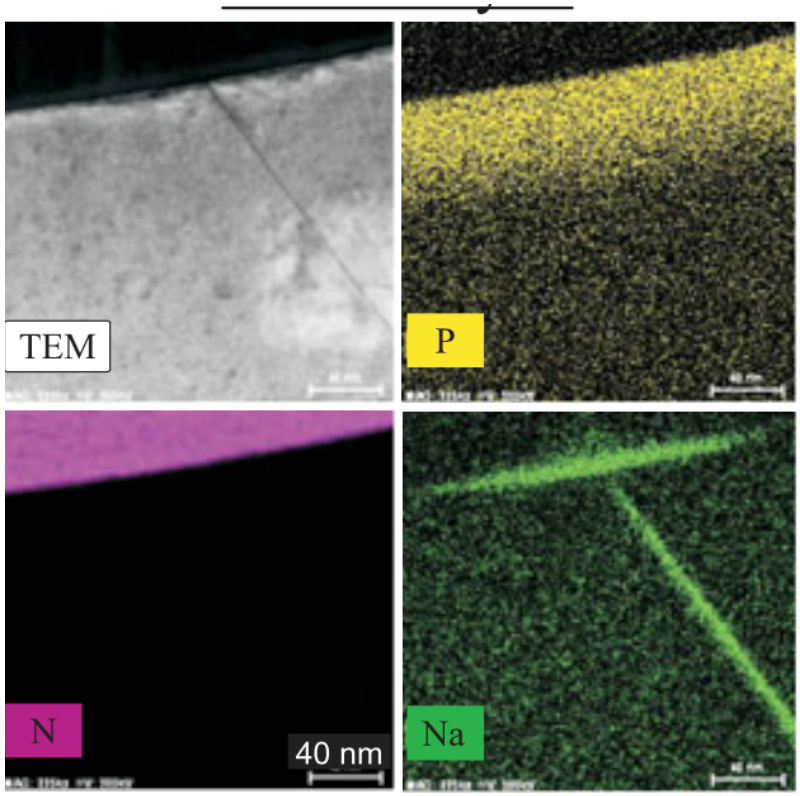


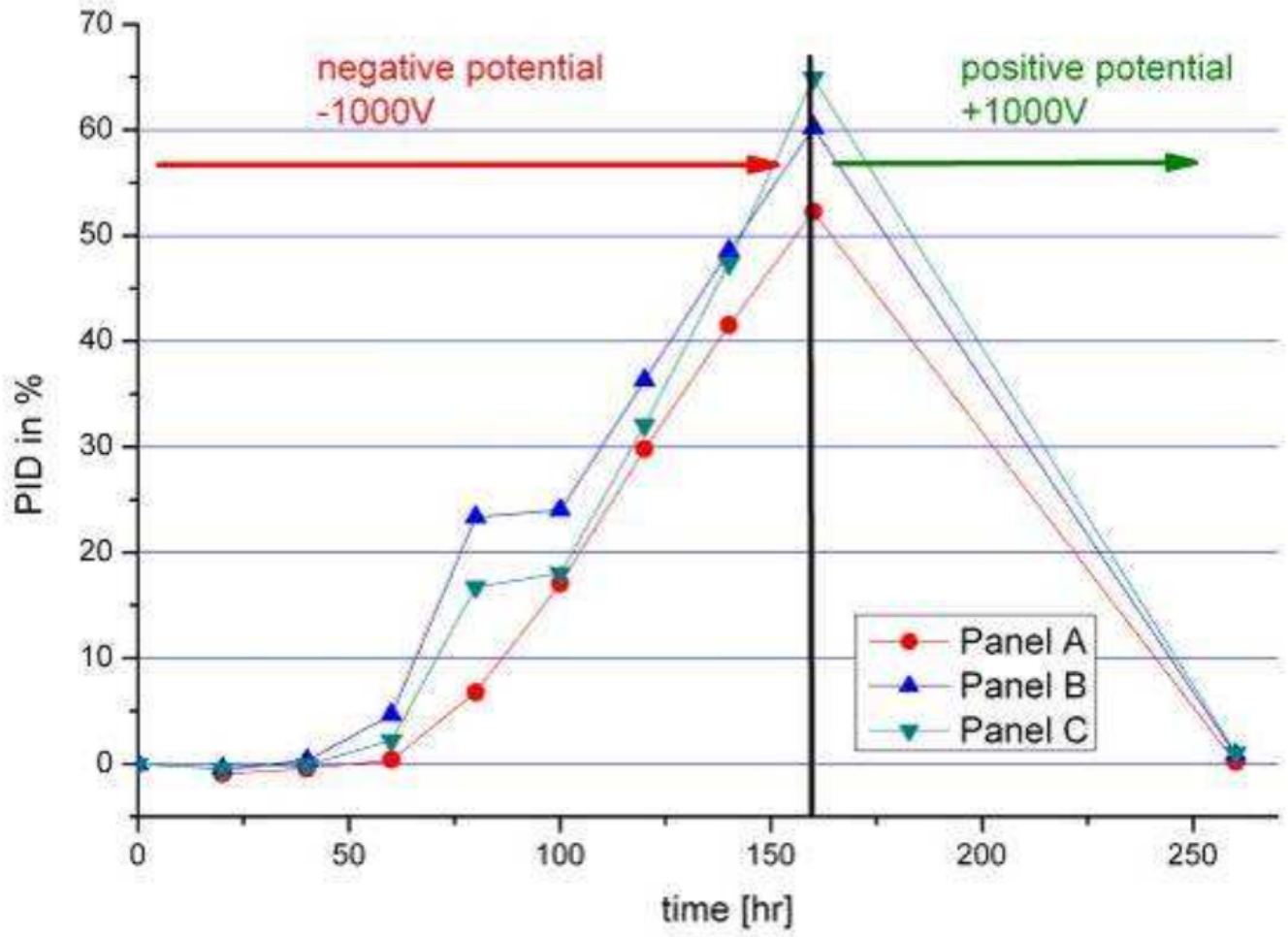


Lausch et al., IEEE Journal of Photovoltaics 2014

Explaining PID

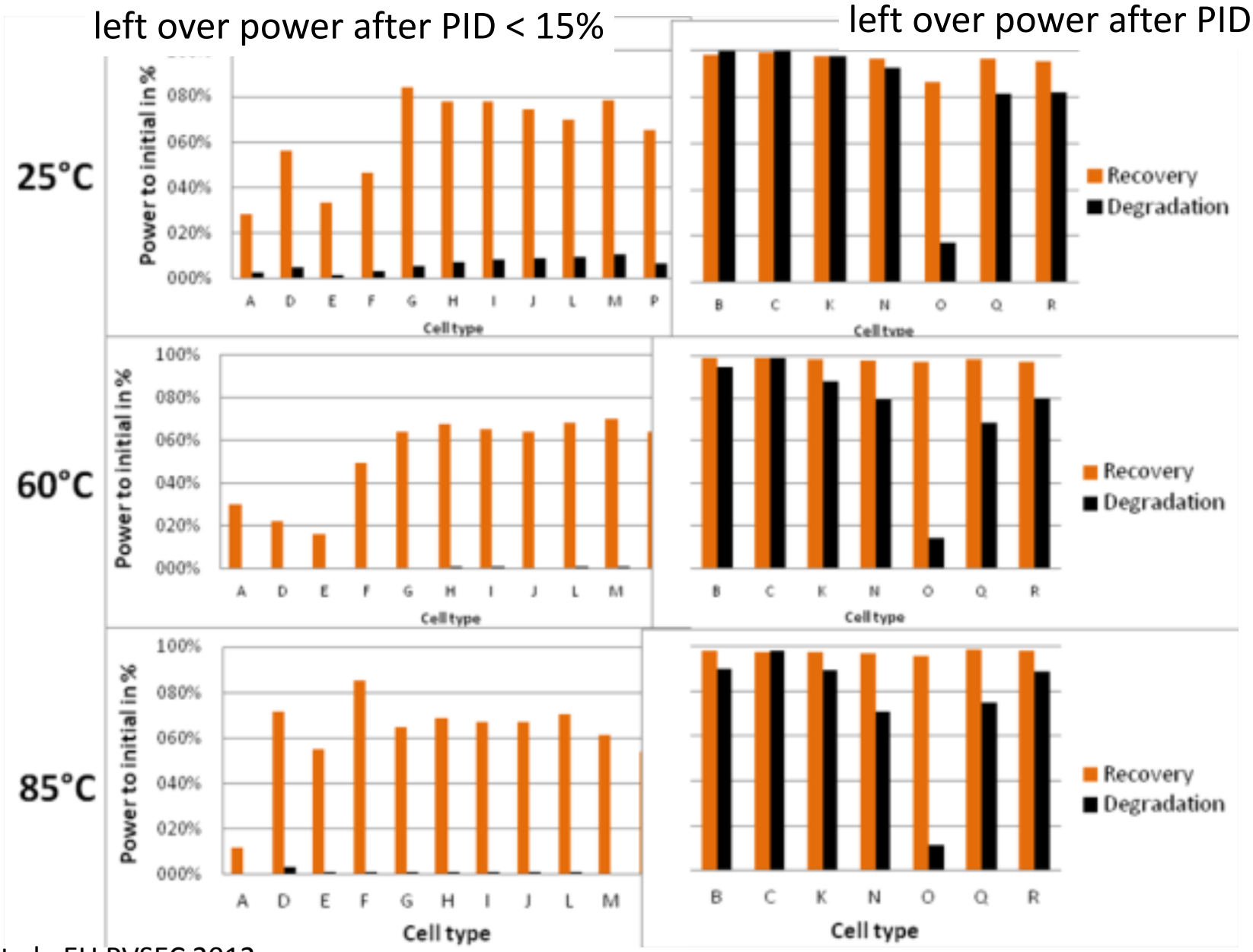
- Under wet (snow, humid and dusty, ….) conditions, the glass is at ground potential leading to high electric field towards the cell.
- Na^+ ions from the glass migrate to the cell through encapsulant and SiNx (ARC).
- Decoration of defect in silicon by Na^+ leading to shunts and PID.
- The role of humidity (+dust) is to spread the ground contact on the glass surface. Closer to the frame, PID is more severe.
- The ion mobility in glass and encapsulant enhances with temperature. Activation energy of the PID is seen to be close to that of ion transport in glass in many cases.
- Localized poor contact between encapsulant and the ARC result in nonuniform PID even in lab tests.

PID recovery



Pingel et al., EU PVSEC 2010

PID Recovery



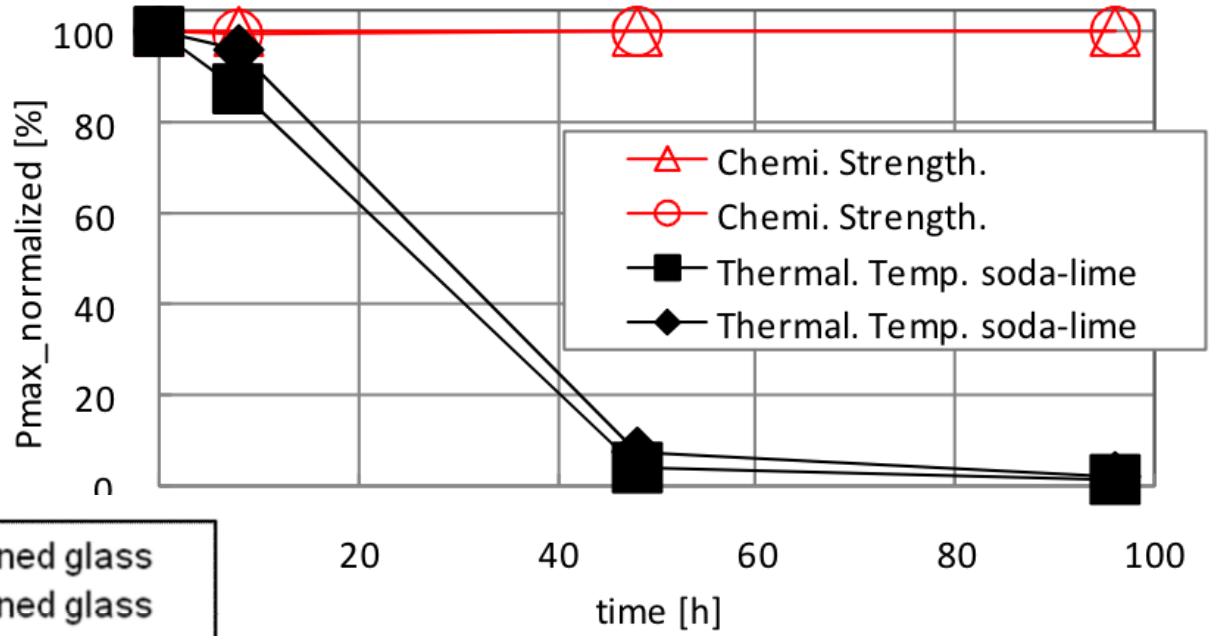
Koch et al., EU PVSEC 2012

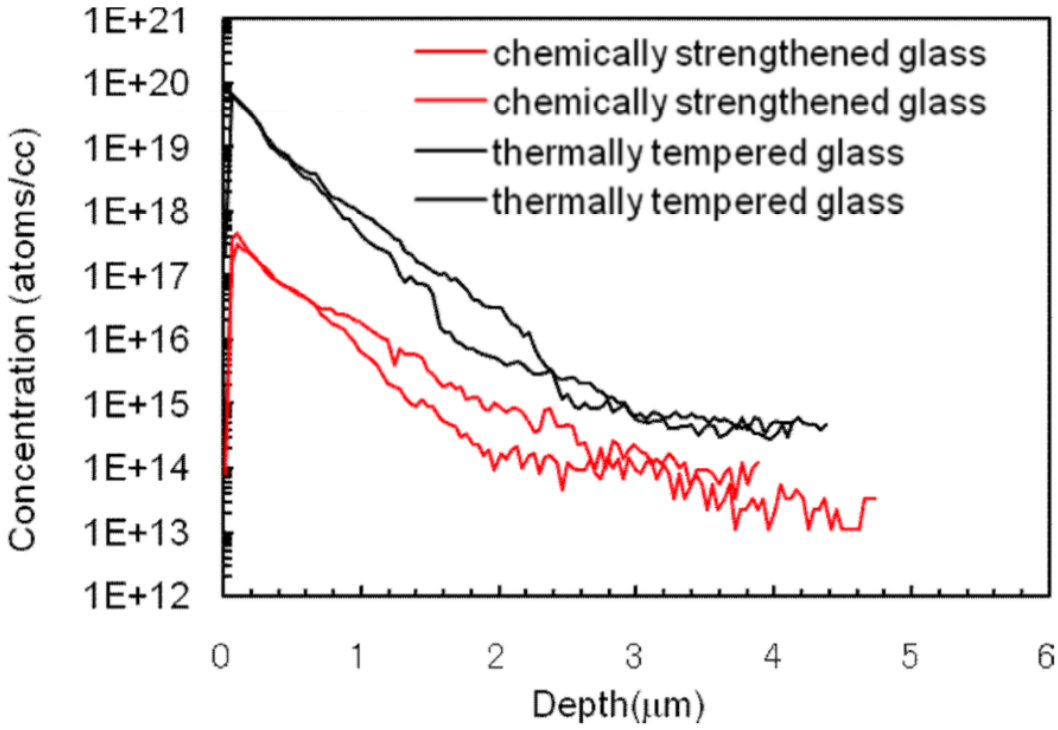
PID – Mitigation Strategies

- Due to large negative potential resulting in Na+ transport from the glass through the EVA and ARC to the cells
- Accelerated by temperature and humidity – out of our control in field
- Would be smart not to count on recovery
- Mitigation:
  - **Keep the modules clean (maintenance)**
  - **Operate strings with only positive and ground (system level)**
  - **Reduce sodium in glass or add barrier layers in glass (module)**
  - **Increase the sodium transport resistance of encapsulant (module)**
  - **Increase the sodium transport resistance of SiNx (cell level)**
  - **More robust emitter design and use of low defect silicon (cell level**)

Modification of glass

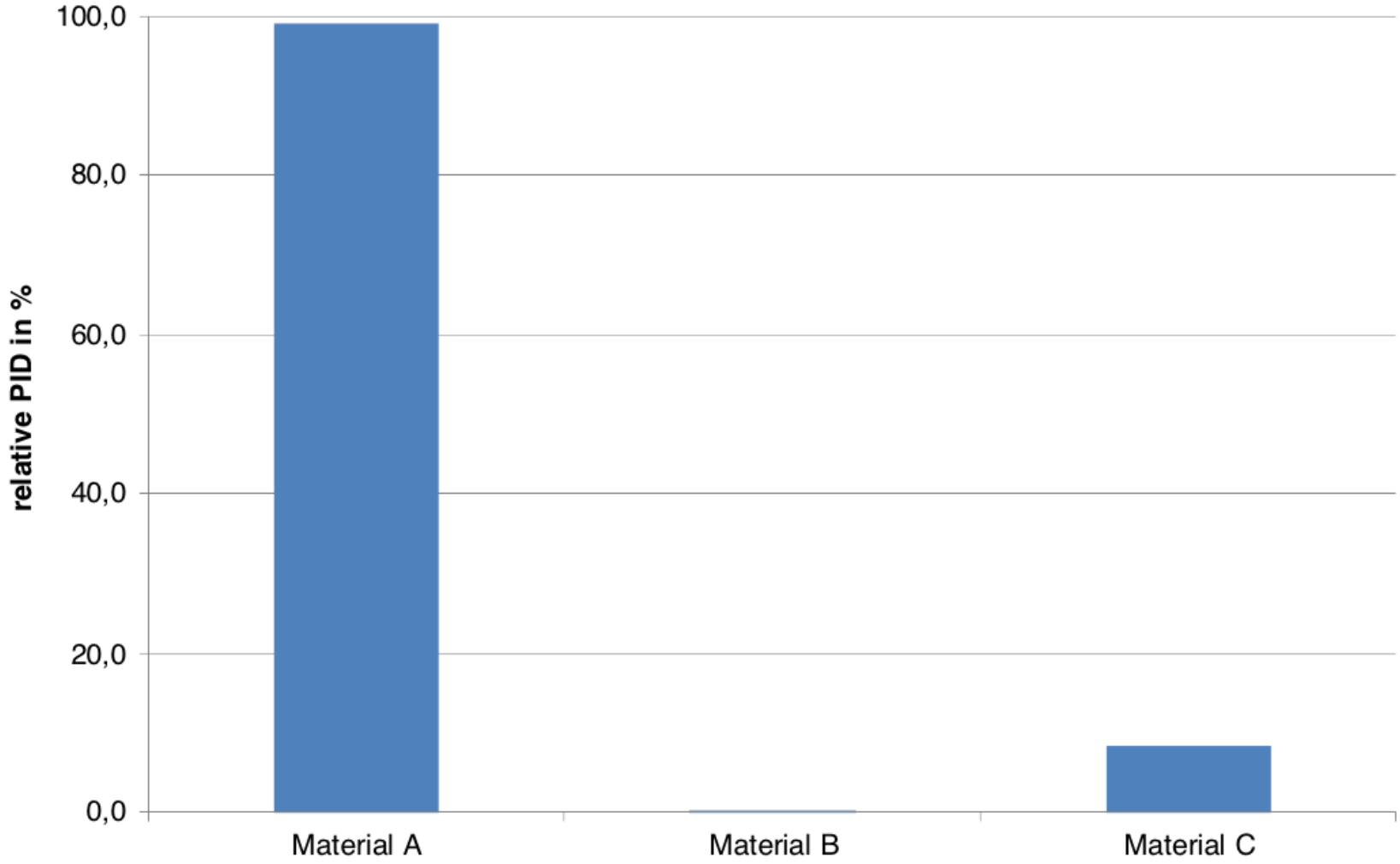
- Na replaced with K at the surface of the glass
- Resistivity increases by 2 to 3 orders of magnitude





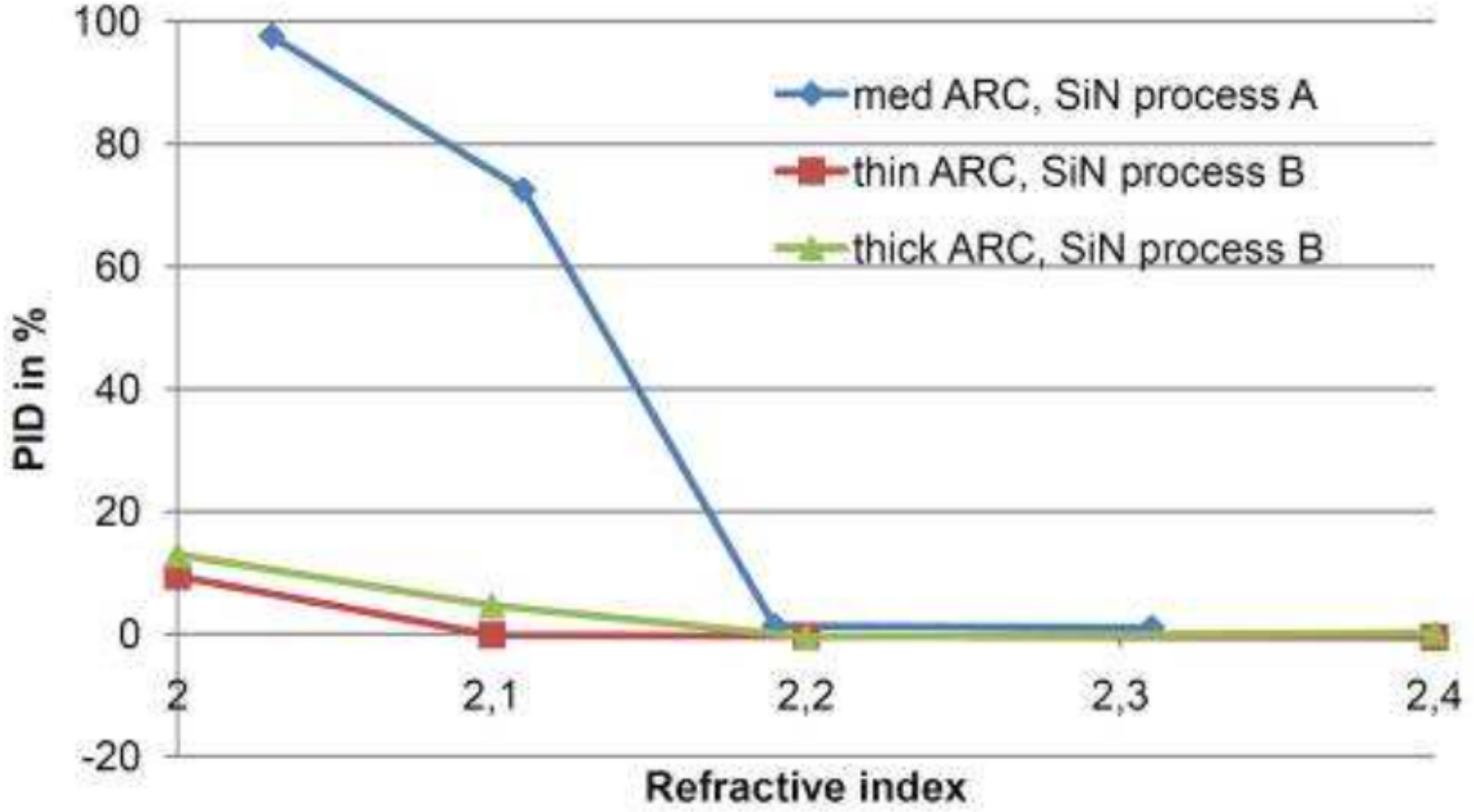
Kambe et al., IEEE PVSC 2013

Impact of encapsulant



Pingel et al., EU PVSEC 2010

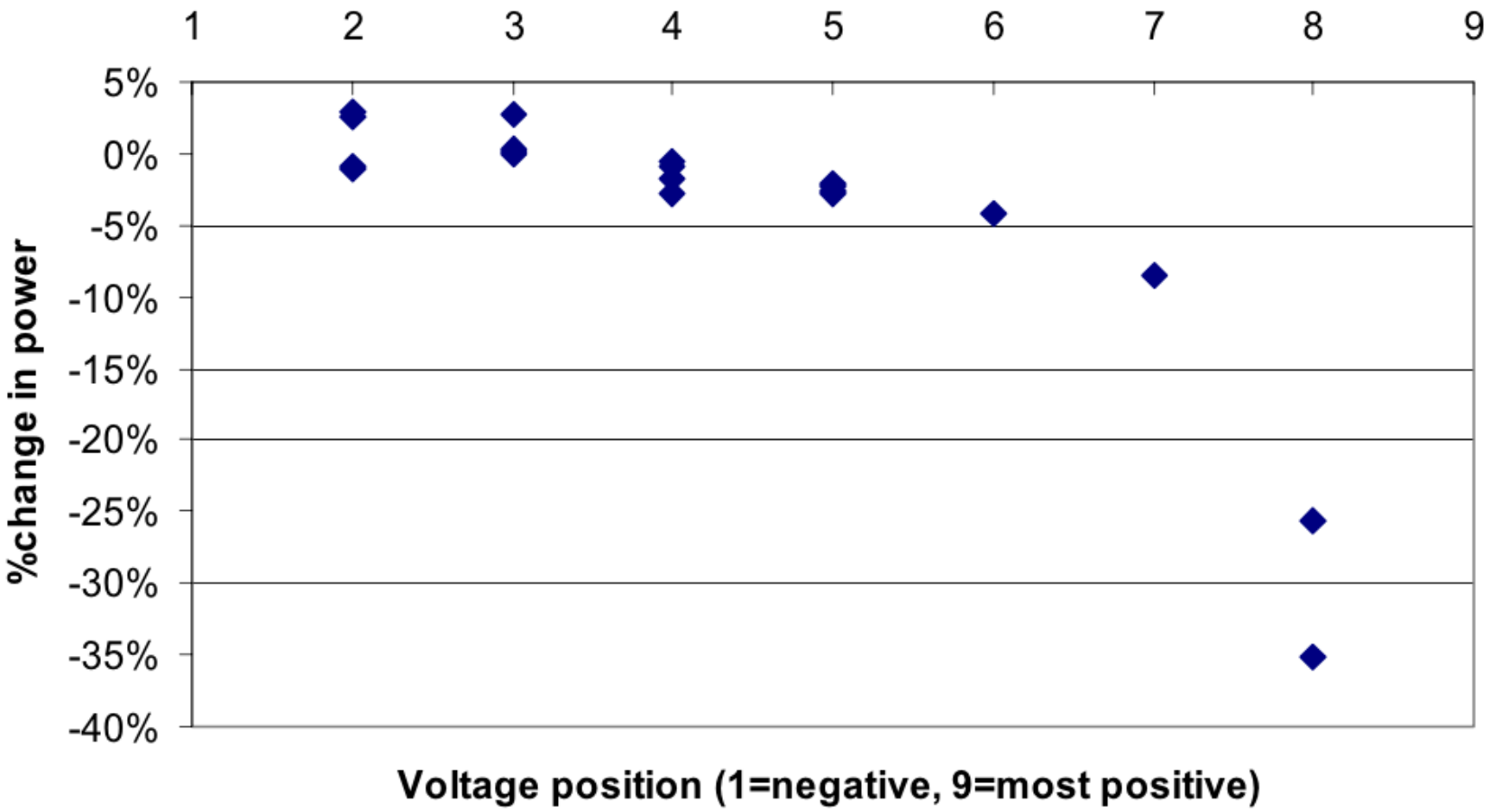
Impact of SiNx ARC



Pingel et al., EU PVSEC 2010

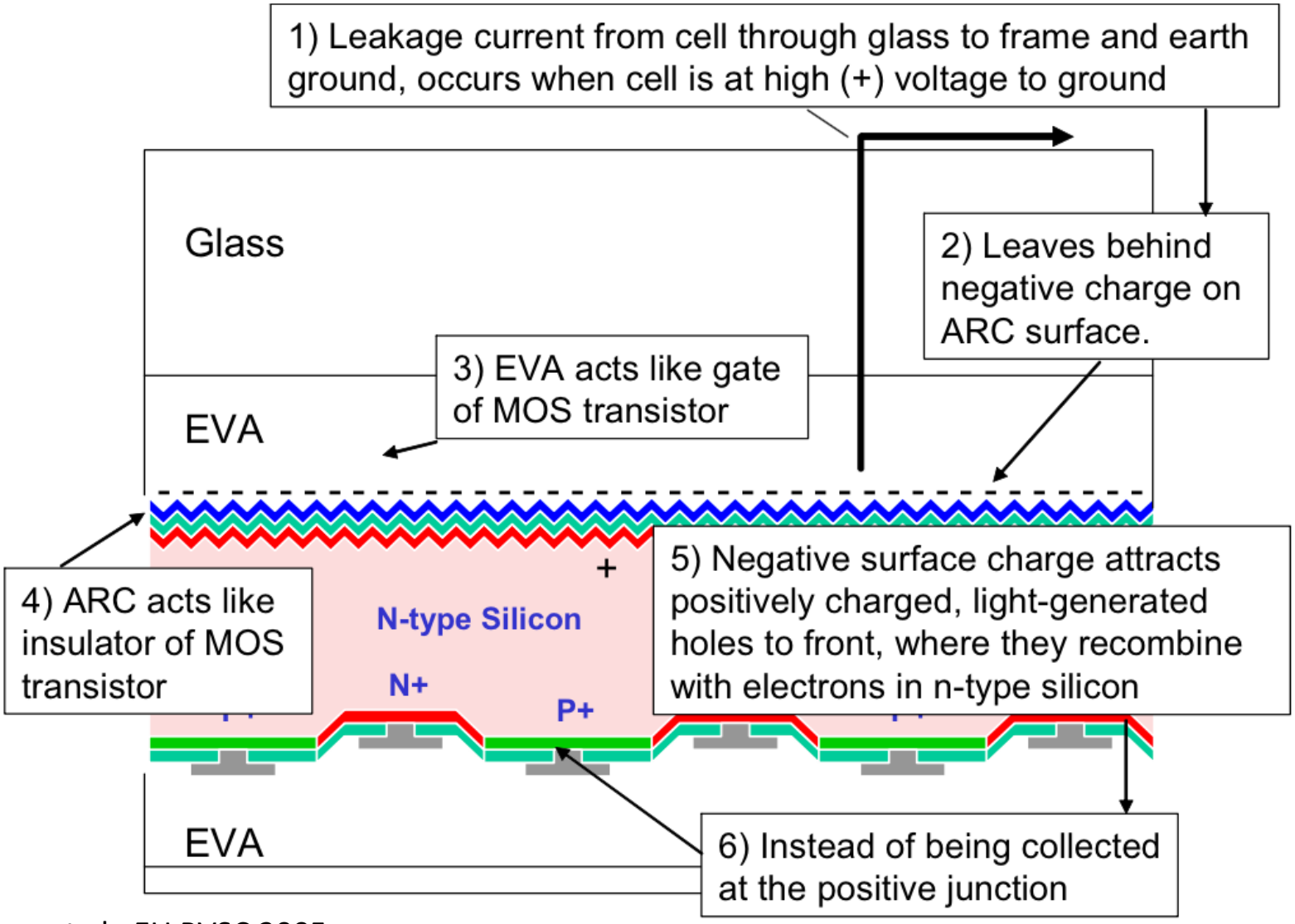
What about positive polarity?

Positive polarity stress on cells



Swanson et al., EU PVSC 2005

PID in positively biased cells



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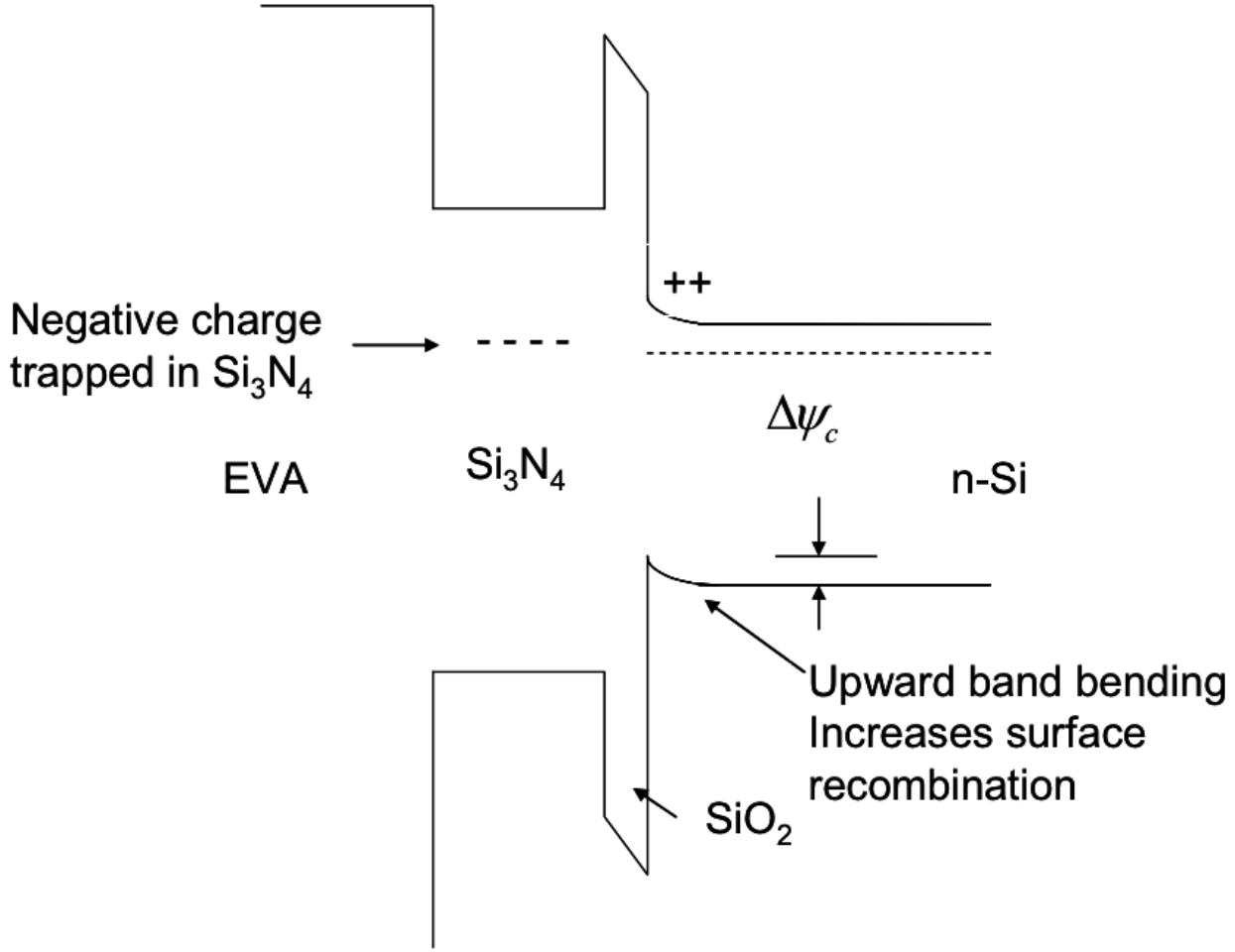
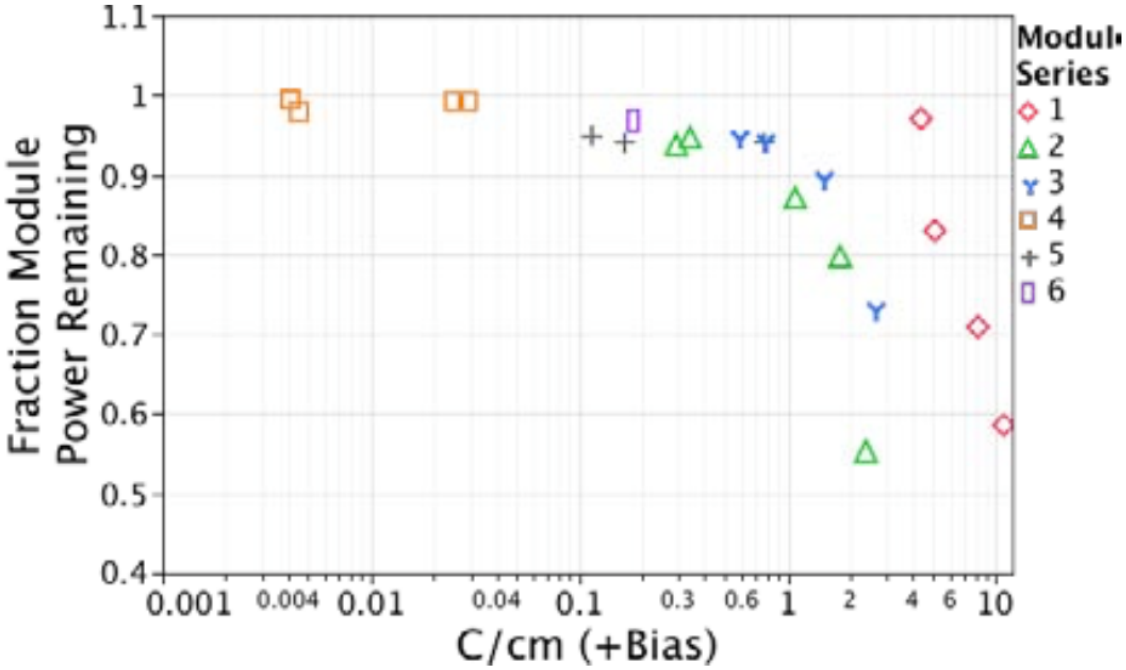


Recovered by UV irradiation.

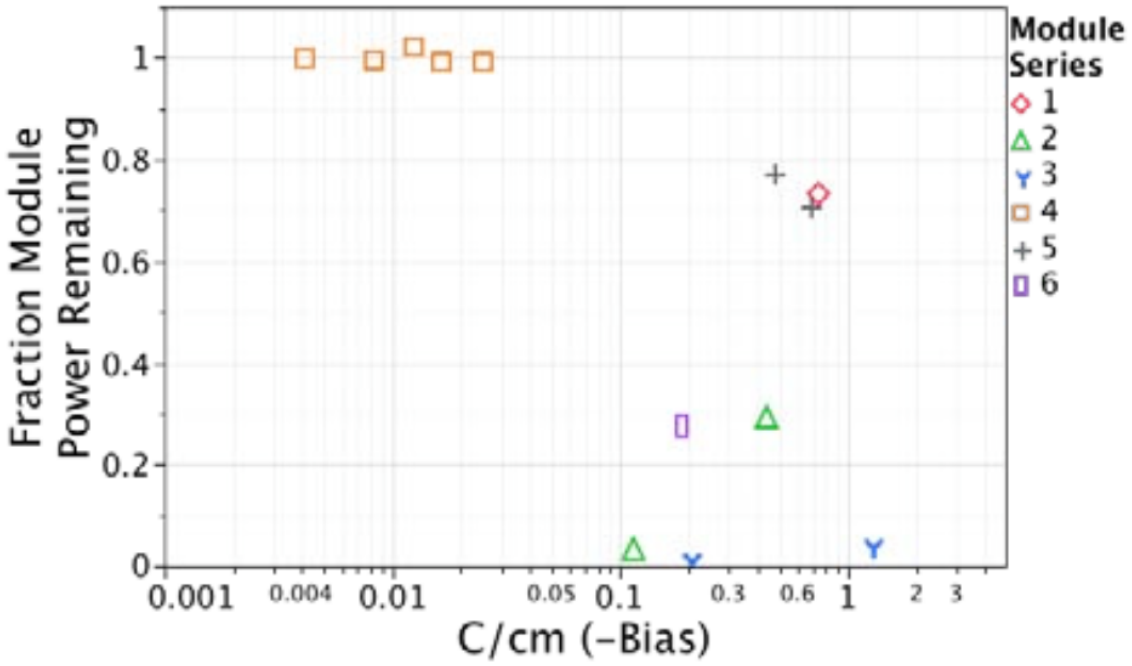
Swanson et al., EU PVSC 2005

PID

Positive stress



Negative stress



Hacke et al., 2010 EU PVSEC

PID – Test standard

- IEC 62804 is under preparation
- Draft test procedure
  - Chamber air temperature 60 °C ± 2°C
  - Chamber relative humidity 85 % ± 5 % RH
  - Test duration 96 h
  - Voltage: module nameplate rated system voltage (e.g.: 1000 V), 2 for each polarity, 1 module supplied for control, voltage applied during temperature ramps
  - Pass criterion: both modules of a tested polarity must show < 5% power degradation and pass IEC 61215 ed. 2 visual inspection criteria

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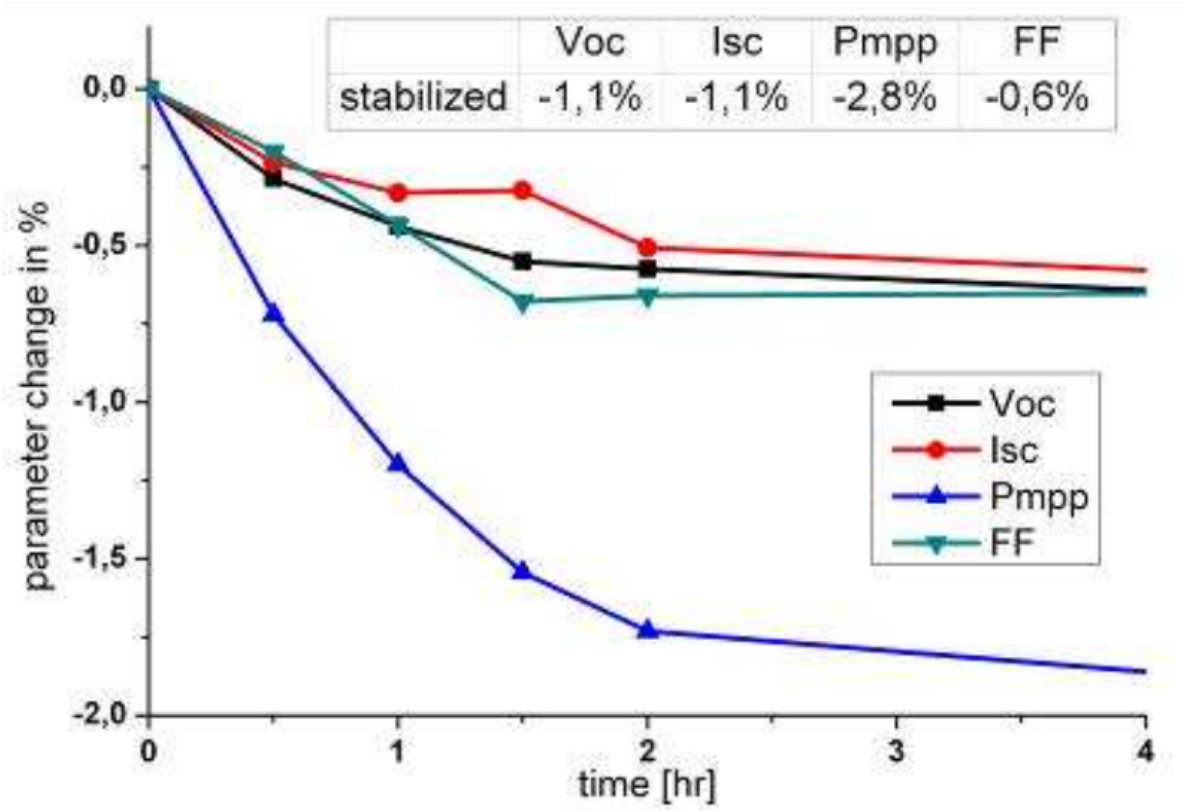
What is LID?

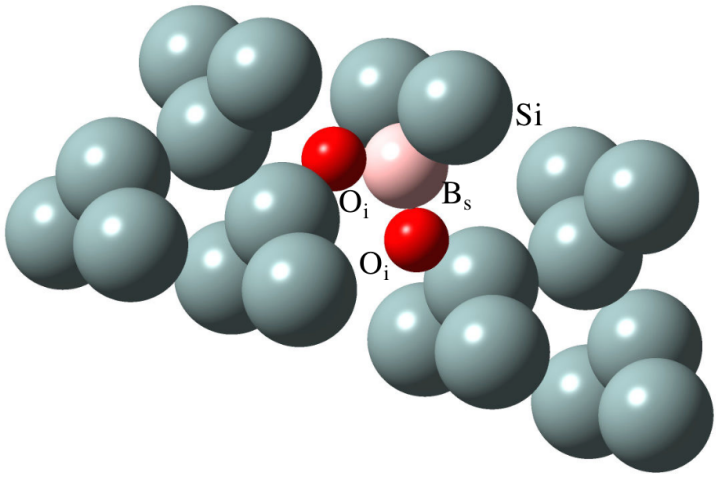


Performance of cells and modules is seen to degrade at a fast rate during the initial operation.

Pingel et al., EU PVSEC 2010

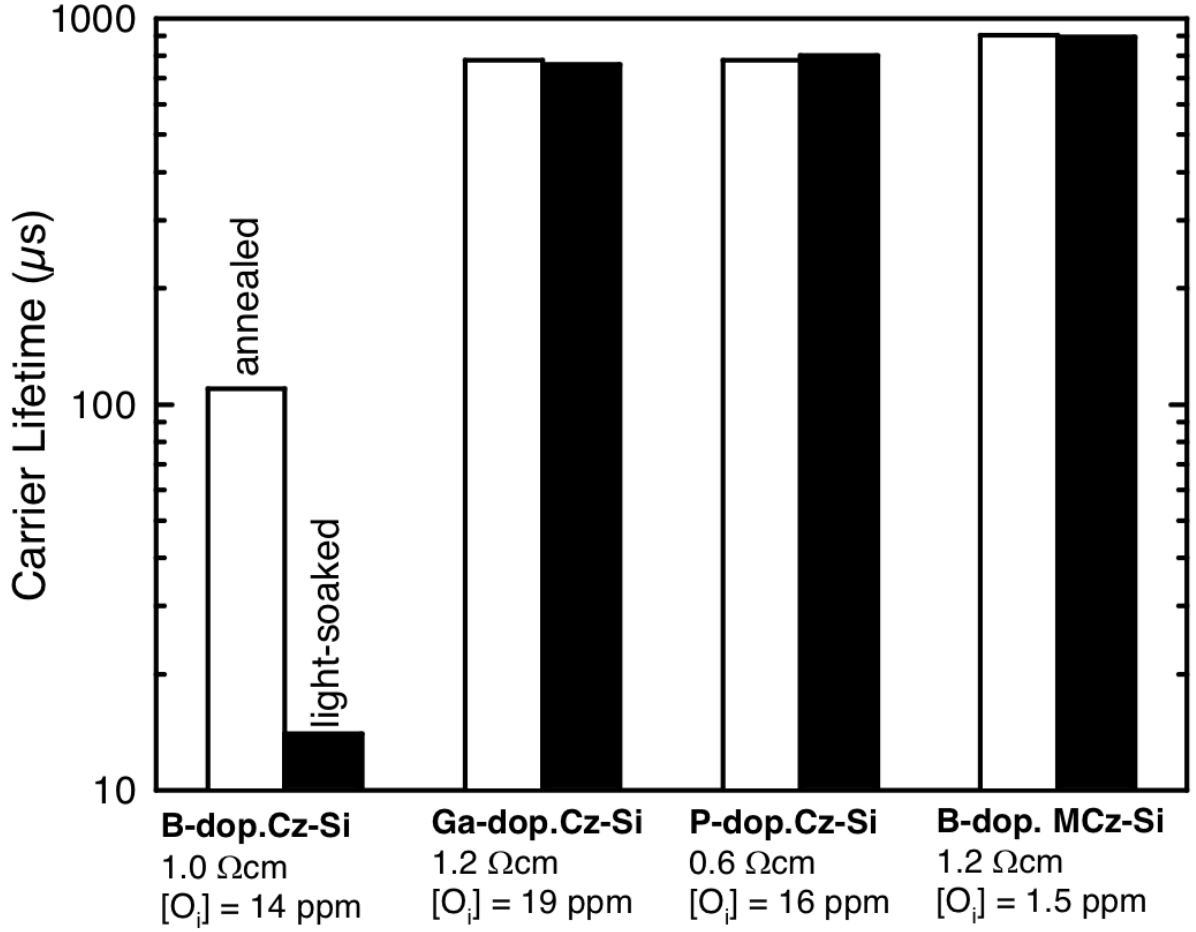
LID mechanism

- Formation of B_sO_{2i} due to illumination
- This defect introduces electronic states in the middle of the bandgap of silicon ($E_C - 0.4$)
- Results in lower minority carrier lifetime



Schmidt, Solid State Phonomena, vol. 95-96, pp. 187-196, 2004

LID mechanism



No degradation in Ga doped p-type Si and n-type silicon.

Schmidt, Solid State Phonomena, vol. 95-96, pp. 187-196, 2004

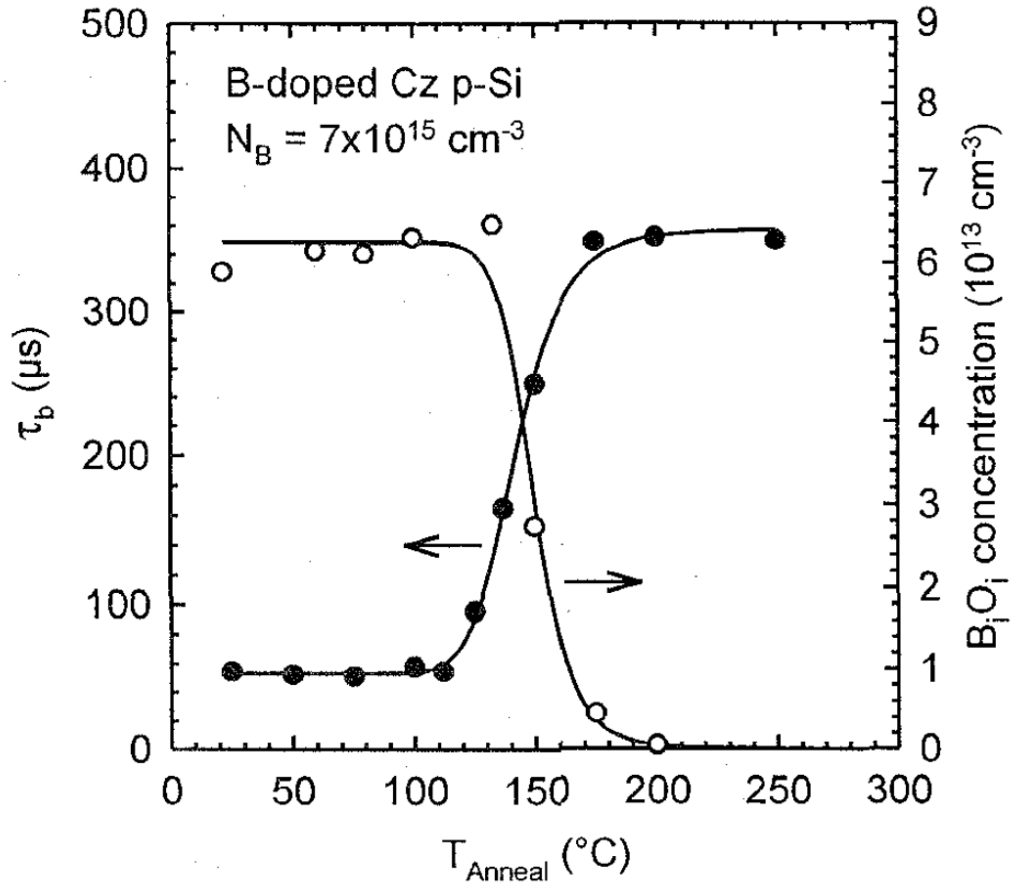
LID mechanism

Silicon type	Average LID of cell batches			
	Mean	Median	Min	Max
Mono	2,1%	1,8%	0,3%	5,1%
Multi	1,5%	1,4%	0,6%	3,5%
Multi UMG	4,0%	4,0%	1,9%	6,7%

CZ mono wafers have higher concentration of oxygen than multi wafers.

Pingel et al., EU PVSEC 2010

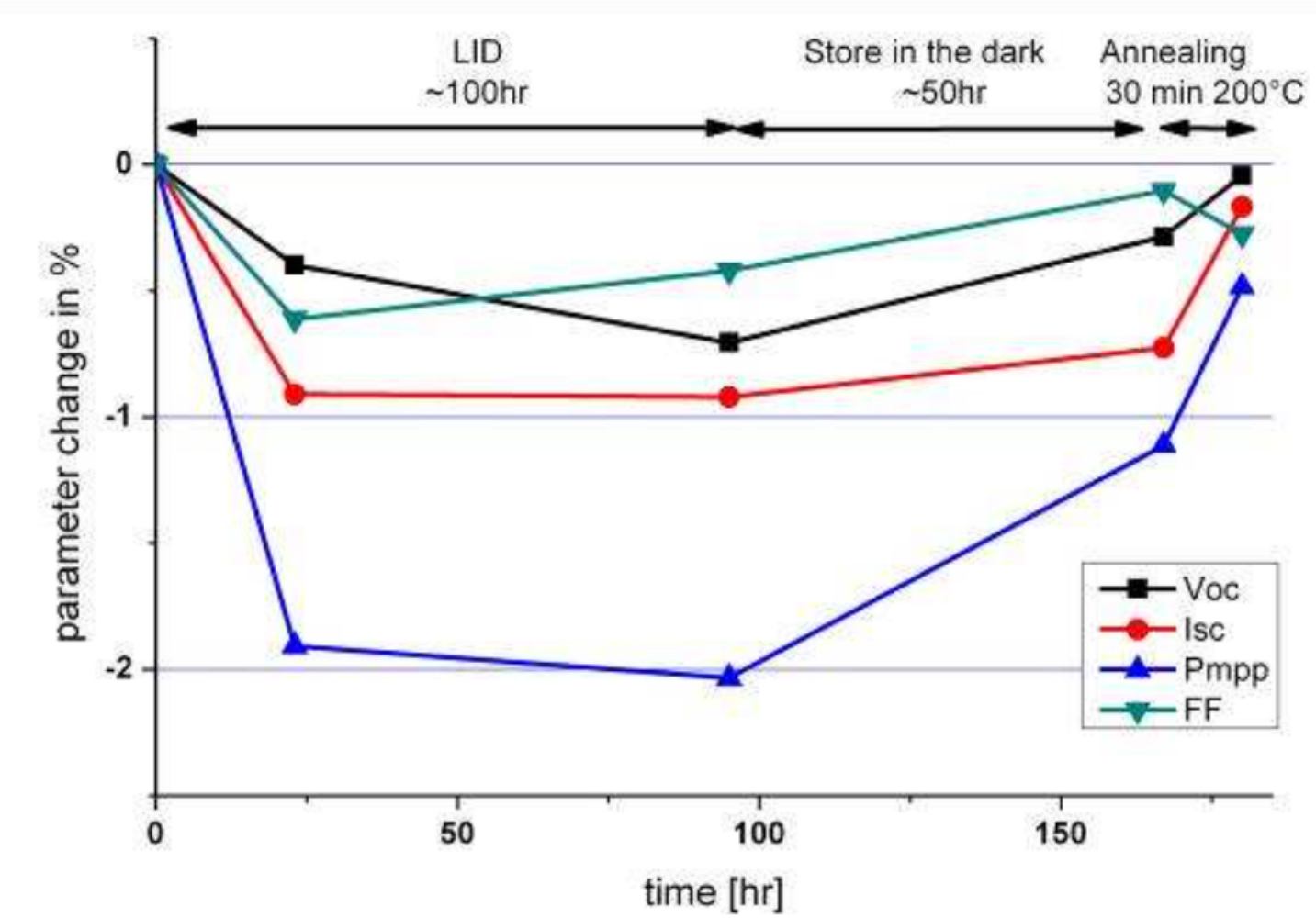
Recovery of LID



Thermal annealing at 200 C or higher should recover the performance.

Schmidt et al., IEEE PVSC 1997

Recovery of LID (2)

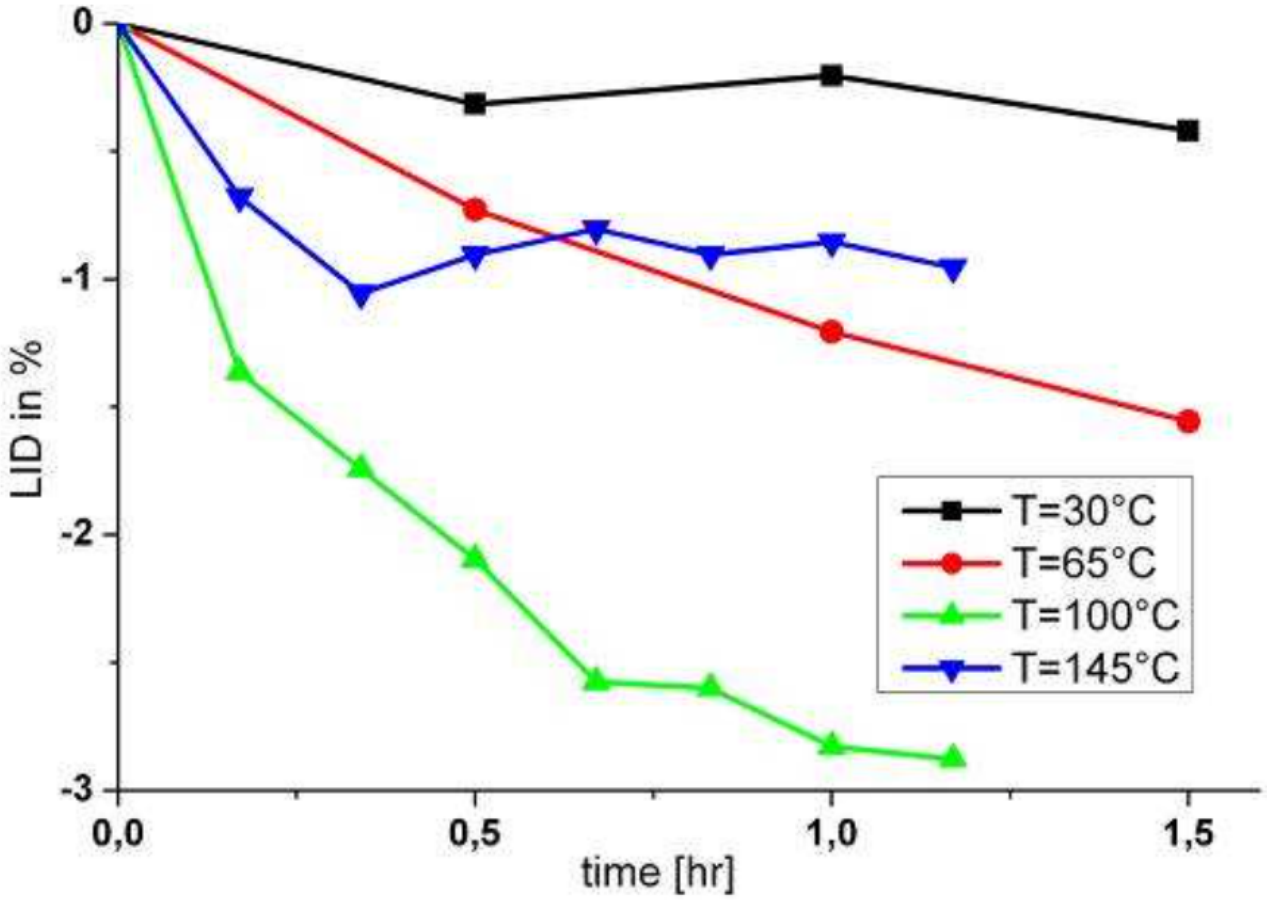


Pingel et al., EU PVSEC 2010

LID – Mitigation Strategies

- Industry long term perspective
  - Move to n-type wafers
- Short term perspectives?
  - Quality checks
  - IEC 61215 specify light socking but no temperature

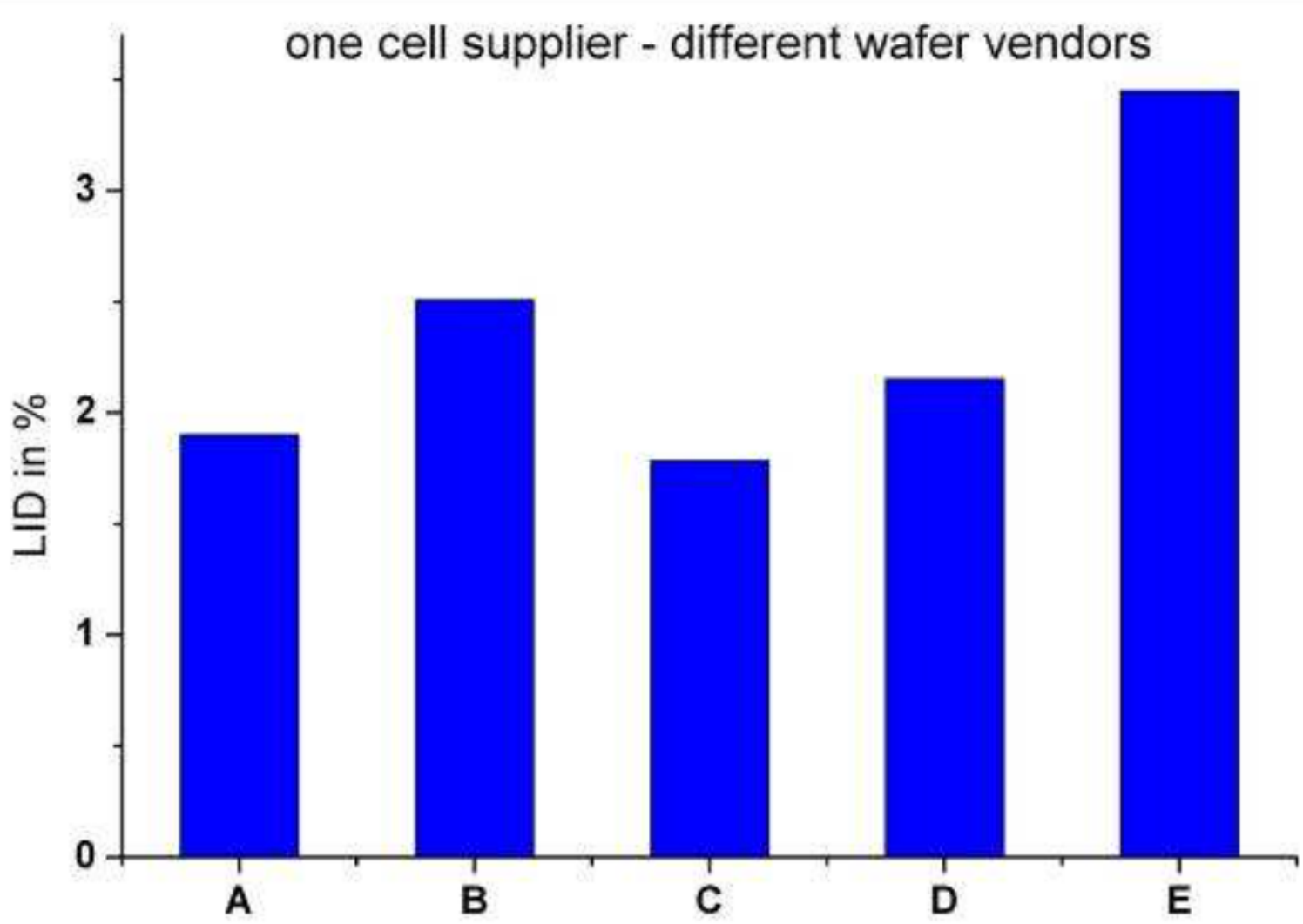
LID – Mitigation Strategies: Points to ponder



Temperature of light soaking should be specified.

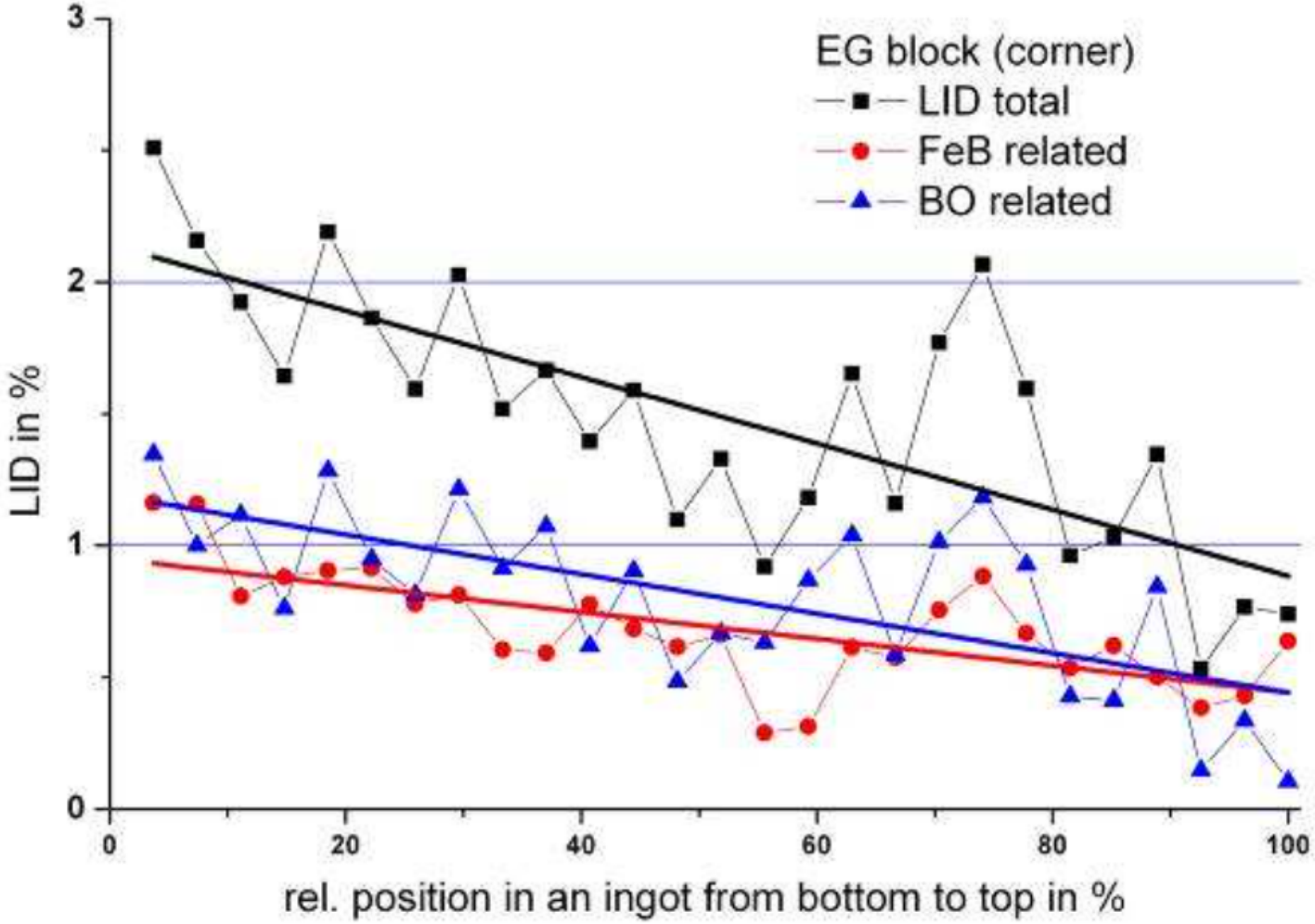
Pingel et al., EU PVSEC 2010

LID – Mitigation Strategies: Points to ponder



Pingel et al., EU PVSEC 2010

LID – Mitigation Strategies: Points to ponder



Pingel et al., EU PVSEC 2010

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